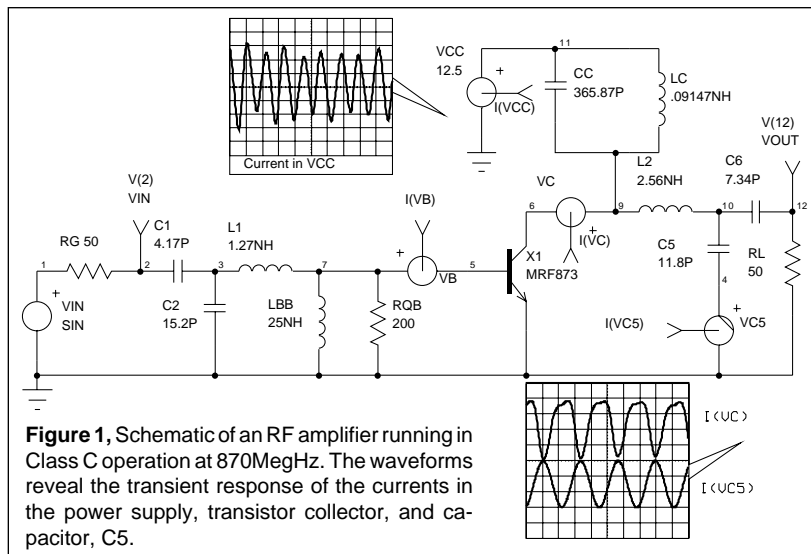# Simulating Class C RF Amplifiers

SPICE can be a versatile tool for RF work as long a few simple precautions are taken. Significant parasitics must be included in the circuit description, models of active devices must be represented using subcircuits, and selection of transient analysis options must be considered. The transient options include the total analysis time, the data printout step and delay, and the simulator error tolerances. Of course, SPICE will also do AC analyses of RF circuits, but this is not its strong suite as many other simulators will also do linear small signal work. The real strength SPICE based simulators, such as IsSPICE3, is in its time domain capability where either repetitive or non-repetitive waveforms can be used as stimulus. This ability is handy for burst work, measurement of peak stresses under normal operation or momentary fault conditions, detailed study of bypass networks, and many other conditions. Since test points do not load the circuit in any way, measurements that would be impossible on the bench can be easily made with the IsSPICE3 simulation.

Figure 1, Schematic of an RF amplifier running in Class C operation at 870MegHz. The waveforms reveal the transient response of the currents in the power supply, transistor collector, and capacitor, C5.

Shown in Figure 1 is a typical circuit used to simulate the operation of a class C power device. The device used here, X1, is the Motorola MRF873 NPN power BJT. It can produce 15 watts of output power in the 806-960 megahertz range. RG provides 50Ω impedance for the generator. C1, C2, and L1 are

used for input matching. LBB and RQB are for DC return to ground and Q limiting for the base. L2, C5, and C6 are used for output matching. CC and LC form a return to VCC for the collector. RL is 50Ω. The generators VB, VC, and VC5 are zero valued sources used to measure the instantaneous circuit currents.

A typical simulation of Figure 2 requires 23.6 seconds on a 486/33 (RELTOL=.0003) using IsSPICE3, a new SPICE simulator based on Berkeley SPICE 3E.2. The change in RELTOL was required for increased accuracy, although the default of .001 provided comparable results. At 870 megahertz one cycle takes about 1.1ns. Since class C circuits need some number of cycles to stabilize, this circuit was simulated from T = 0ns to T = 20ns with output data accumulated from 15ns to 20ns. The simulation has about 15 cycles to settle before data is gathered and is pretty well settled by that time.

After initial testing of a nominal case (VCC=12.5, Power In=3W) the parameter sweeping features of IsSPICE3 were used to sweep the input power. The input power is controlled by the voltage of VIN. In order to easily control the simulation parameters, a simple subcircuit was made to convert input power in watts to the peak voltage required by the IsSPICE3 voltage source. The power supply, VCC, was also made a variable. The conversion is shown below.
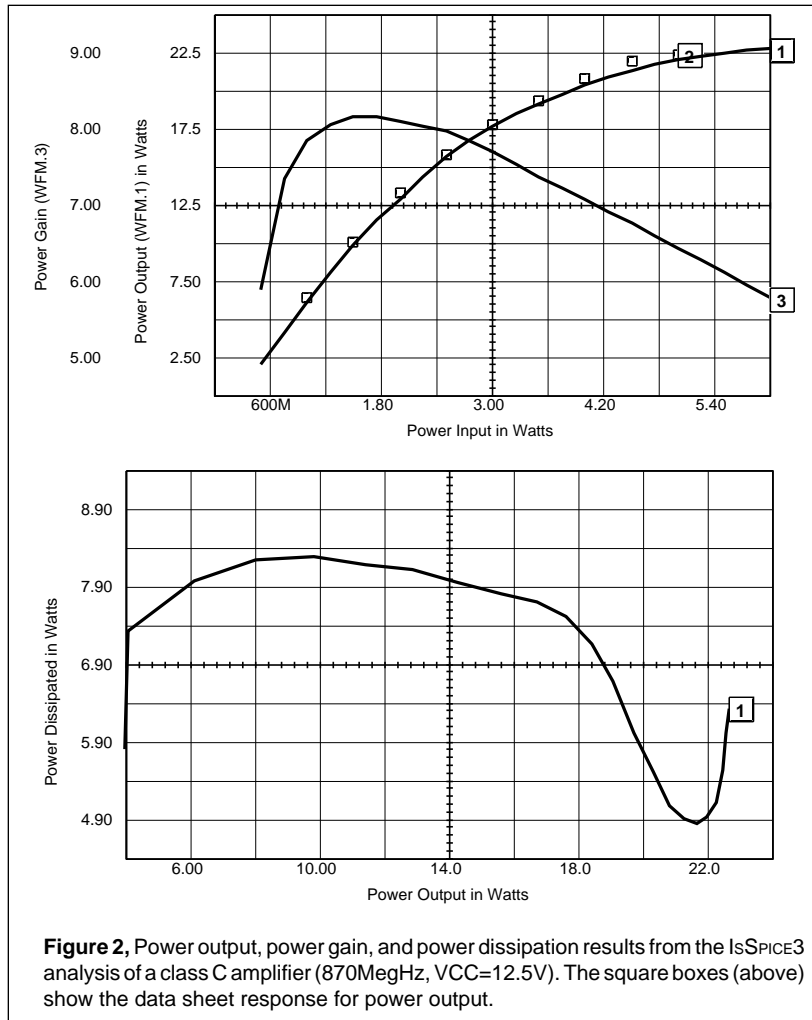
Replace:	With:
VCC 11 0 12.5	VCC 11 0 VTEMP
VIN 1 0 SIN 0 Vpeak 870 .5N	X2 1 0 VSIN {PIN=PTEMP}
	.SUBCKT VSIN 1 2
	VIN 1 2 SIN 0 {(PIN*50)^.5*2*2^.5} 870 .5N
	.ENDS

After setting up the extended syntax, the control statements

    *OPT VTEMP=5 TO 17 STEP=.25   and
    *OPT PTEMP=.5 TO 6 STEP=.25

can then be used to sweep the parameters VTEMP (equal to the power supply voltage) and PTEMP (input power in watts).
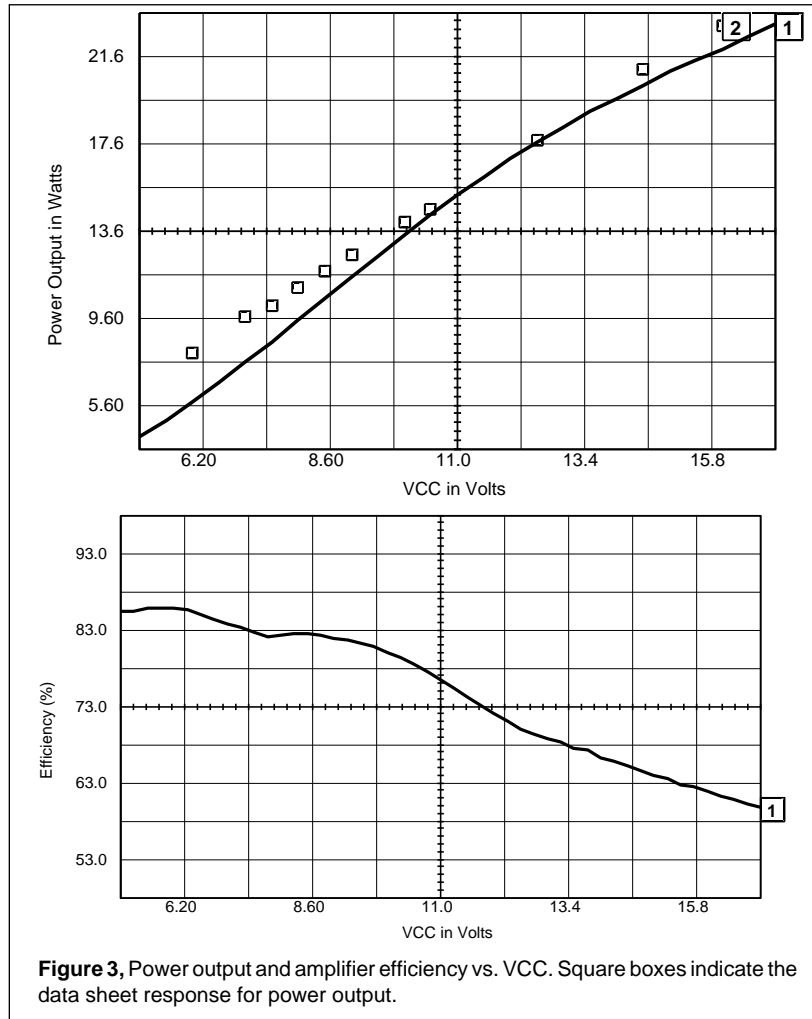
During the simulation the waveforms at various points were sampled. INTUSCOPE, a SPICE data post processor, was used to reduce the IsSPICE3 voltage and current data into output power and DC power values. After the sweep, INTUSCOPE then calculated the power gain (10*lgt(Pout/Pin)), efficiency (Pout/Pdc), and dissipation (Pout-Pdc). Since there is no circuit loading associated with monitoring voltage and current, mea-

Figure 2, Power output, power gain, and power dissipation results from the IsSPICE3 analysis of a class C amplifier (870MegHz, VCC=12.5V). The square boxes (above) show the data sheet response for power output.

surement of the capacitor RMS current and peak voltage is possible. For nominal power input, the peak-peak voltage across C5 was 93.00V, while the RMS current was 2.082A. This type of data is vital for making informed component selection decisions.

Figure 2 (top graph) shows the excellent tracking between the IsSPICE3 simulation and the data sheet values for output power and power gain vs. input power. The lower graph contains the results for the power dissipation in the MRF873. Figure 3 shows the simulation results for efficiency and output power vs. VCC at constant input power.

Figure 3, Power output and amplifier efficiency vs. VCC. Square boxes indicate the data sheet response for power output.

```
.SUBCKT MRF873 1 2 3
LC 1 4 0.50E-9
LB 2 6 1.02E-9
LE 5 3 0.07E-9
CC 4 3 15.0E-12
CB 4 6 1.00E-12
Q1 4 6 5 QR01
.MODEL QR01 NPN (BF=98  VAF=150  VAR=10.0  RC=.15 RB=1.43 RE=.26
+ IKF=1.0 ISE=7.6E-14 TF=1.2E-11 TR=1.7E-09 ITF=1.7 VTF=5.3
+ CJC=10.7E-12 CJE=36E-12 XTI=3.0 NE=1.5 ISC=2.4E-14 EG=1.11
+ XTB=1.5 BR=2.29 IS=8E-15 MJC=0.33 MJE=0.33 XTF=4.0 IKR=0.5
+ KF=1E-15 NC=1.7 RBM=1.02 IRB=1.60E-02 XCJC=0.5)
.ENDS
```

Table 1, The SPICE subcircuit netlist for the MRF873 RF power transistor. Connections are Collector(1), Base(2), Emitter(3). The subcircuit may be used with any SPICE simulator.
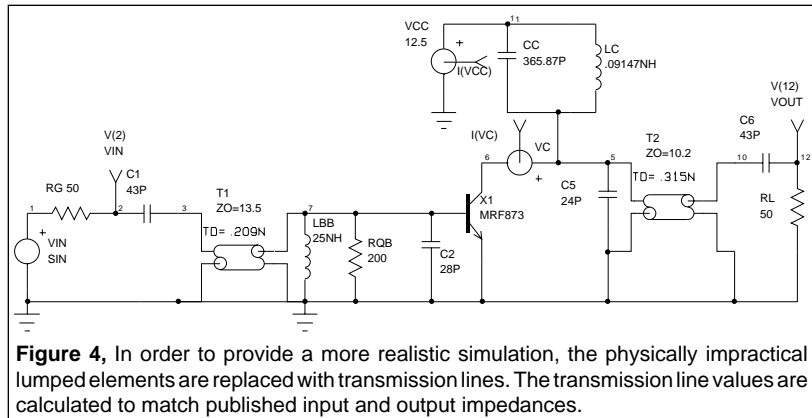
Figure 4, In order to provide a more realistic simulation, the physically impractical lumped elements are replaced with transmission lines. The transmission line values are calculated to match published input and output impedances.

Once the relationships were studied and a final output power and VCC range were selected for detailed analysis, the physically impractical and somewhat narrow bandwidth lumped element networks in Figure 4 were replaced with transmission lines. The t-line values were calculated to match published input and output impedances. Other values were taken from the Motorola data sheet. The simulation results obtained were more accurate but still within 10% of the lumped element approach. SPICE 2G.6 based simulators have trouble running circuits containing ideal transmission lines with time delays that are short relative to the total analysis time. However, new algorithms in Berkeley SPICE 3E.2 and IsSPICE3 allow ideal transmission lines to be simulated orders of magnitude faster that SPICE 2 based versions. For example, the simulation of Figure 4 took 521.85 seconds on a popular evaluation version of a PC SPICE program based on SPICE 2G.6. IsSPICE3 simulated the same circuit in 41.25 seconds (486/25). In addition, IsSPICE3 includes two types of lossy transmission lines. Based on the comparable run times and results achieved either approach, lumped element or transmission line, is acceptable for simulation purposes. The complete set of simulations contained in this article is available on floppy disk from Intusoft (222 West 6th St. San Pedro CA. 90731, 310-833-0710, Fax 310-833-9658) for a nominal charge.

From the accurate results presented here, it is clear that simulation of class C RF circuits using SPICE is practical and productive as long as the circuit and transistors are modeled properly.

Note: Thanks to Bill Sands of **Analog & RF Models**, specialists in the creation of RF device models, (602-575-5323, FAX 602-297-5160) for his substantial contributions to this article.

Article Title: "Simulating Class C RF Amplifiers"

Charles E. Hymowitz
Bill Sands

Abstract: Many designers believe that the analysis of the nonlinear characteristics of class C amplifiers is not practical with popular simulators such as SPICE. However, with the proper modeling of the RF transistors and proper accounting of parasitics, virtually every aspect of the class C amplifier can be studied.

This paper explores some unique techniques and models for simulating amplifiers running in class C operation using the general purpose SPICE circuit simulation program. Results of the simulation of an 870MegHz amplifier including the transient, power gain, power dissipation, power output and efficiency waveforms are given.

Total: 5 Pages, 4 Figures