Receiver construction using 50 ohm modules (gain blocks)

Part 4: 13cm version using a converter

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(First published in the German UKW Berichte journal issue 3/2017)

8. Introduction to the 2300MHz receiver

The receivers already described for 2m, 70cm and 23cm (see Parts 1 - 3) run without any problems and are fun! But a receiver for the 13cm band (2300 to 2450MHz) requires something different because the frequency range of the SDR sticks stops at 1700MHz. A converter for 13cm and beyond using the latest state of the art components must be developed in order to move forward. A detailed Internet search was the starting point to formulate my thoughts. The following details had to be clarified in advance:

a Which one of the existing receivers should be chosen as the IF block for the new converter?

b What conversion local oscillator is required and which frequency range should it cover? Can it be remotely control via USB? Are there suitable and good evaluation boards available to save a lot of development work? What is the highest output frequency required? Does the local oscillator signal need to be filtered before use with the mixer?

c Which down converter should be used? Is there an existing board that is intended for use with an available local oscillator board? What is the highest frequency that the mixer can be used?

d. Which filters are required and still need to be developed?

You can already guess - there is a lot of development work needed!

8.1. The concept of the 13cm converter

The sum of the thinking and the Internet search is summarised in **Fig 41:**

a The IF output of the converter is in the 70cm band. The output centre frequency is f_{IF} = 435MHz. The mixer output is followed by the 70cm bandpass filter from the previous project that passes a frequency range of b = 10MHz (i.e. from 430 to 440MHz).

b The conversion local oscillator required should operate lower than the input signal so that

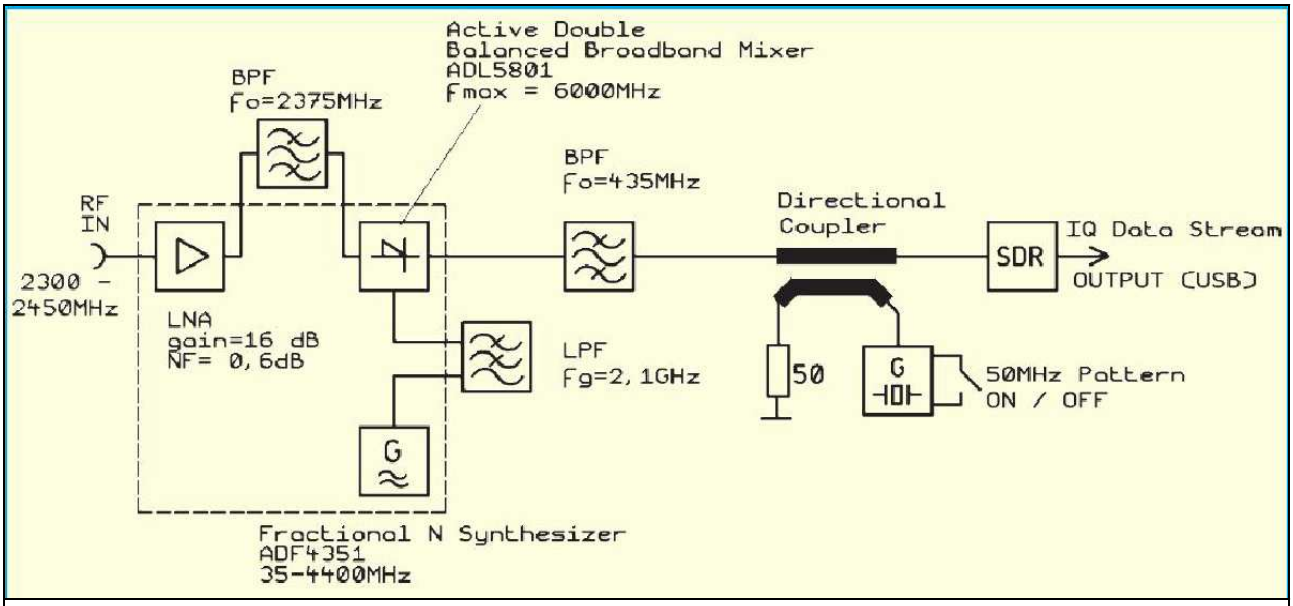

Fig 41: Not elaborate, but a clear concept that builds on existing projects.

the image frequency is at even lower frequencies because the input bandpass filter has increasingly higher stopband attenuation. For receiving the 13cm band (2300 to 2450MHz) this means a centre frequency of the input filter of 2375MHz and a tuning range of the oscillator from 1865 to 2015MHz.

c ANALOG DEVICES supply an evaluation board for the fractional-N synthesiser chip "ADF4352", where a frequency between 50MHz and 4400MHz can be selected via USB. The cheapest, smallest and oldest notebook computer with a USB connection can be used for this frequency setting.

However, the synthesiser must be followed by a filter (here: a 2.1GHz lowpass filter), because Fractional N synthesisers are not always famous for their harmonic purity. Otherwise you will also produce a whole forest of new spurious signals in the mixer

d. Fittingly, ANALOG DEVICES has a "mixer and downconverter board" using the ADL5801 that connects directly to the synthesiser and accepts RF input signals up to 6GHz.

If the receiver with f_{middle} = 1270MHz from the previous project was used as an IF, then with f_{osc} = 4.4GHz then theoretically this would use the maximum input frequency of the converter of (4.4 + 1.27)GHz = 5.67GHz. If the SDR receiver was used at 1.8GHz this would go up to 6.2GHz. That would need a new project with another filter and LNA development. Alternatively using an existing bandpass filter from a previous project for the GPS frequency of 1575MHz, combined with a conversion oscillator frequency of 4.225GHz it would receive 5.8GHz. You see, there are no limits to the imagination here.

The converter itself is installed in a diecast aluminium housing. The input bandpass filter and a lowpass filter (filtering the oscillator signal) are located outside of this housing and connected using SMA cables. It is therefore not possible to switch to other frequency ranges (**Fig 42**).

The low noise preamplifier is shielded in an aluminium housing. It can easily be removed after loosening the SMA connections and replaced if necessary with a version for a different frequency range.

Fig 42: One thing is certain: it is better to have too much shielding rather than too little. Only then can the smallest input levels be reliably received.

8.2. Which microwave CAD program?

The answer is:

Take something that you already know well and whose peculiarities you can always cope with.

But: It should have an almost infinite supply of component models for working at these high frequencies and for all types of microstrip circuits and for all conceivable applications! (All programs can calculate correctly these days)

So the ANSOFT Designer SV (rather than using qucsstudio) was preferred because its complete linear simulator is released with all available models (there are nearly 1000) in the student version and thus fulfils exactly these conditions. The non-linear simulation, the EM simulation and the direct transfer of the simulation into a printed circuit board are removed – but it is still acceptable for private use. This software is only available to download from my homepage plus my tutorial. Ansoft now ignores the existence of this program but has allowed me to host it for the past 10 years for private downloads.

However, it is important to know: using such an expensive professional program the training and operation is much more complex than the "university program" qucsstudio. That's the price you pay.

8.3. The low noise preamplifier (LNA) for 2375MHz

The same basic circuit is used with AGILENT AVAGO's MMGA "MGA-635 P8" as with all previously developed versions for 145/435/1275MHz. However, a data sheet as well as an application note and measurement results are now available in this frequency range from the manufacturer. Despite this the circuit diagram was still being fine-tuned, **Fig 43** shows the result including the changes proposed by AGILENT.

The circuit used in the simulation with the ANSOFT Designer SV is shown in **Fig 44.** It uses the practical values of the coils and capacitors in the RF section and thus all important parameters (NF / S11 / S21 / S12 / S22 / k) were determined. They are compiled together with the measurement results in **Figs 45 to 48.** A very satisfying sight ... because the achieved noise figure NF is 0.6dB, the gain S21 is a good 17dB and the stability k is good up to 10GHz.

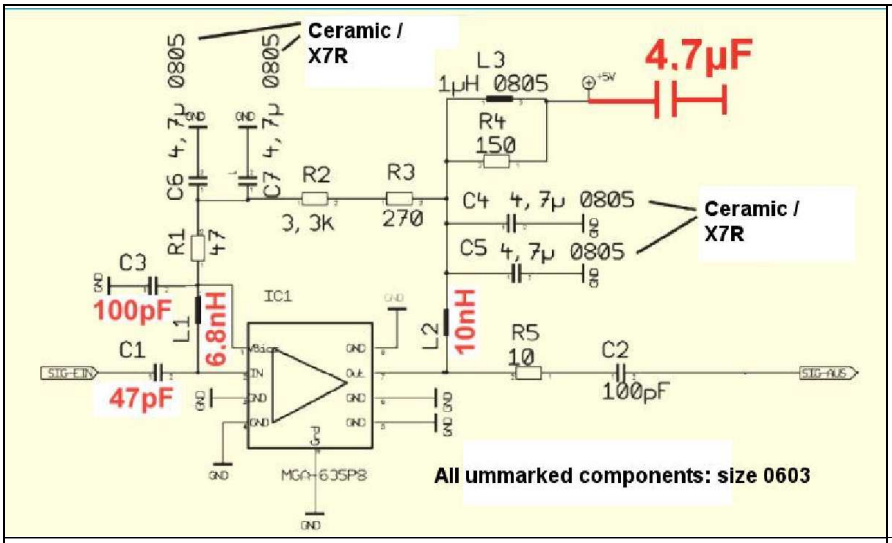

Fig 43: It is good if an already proven circuit and circuit board can be used, then the conversion to 2.3GHz requires less effort.

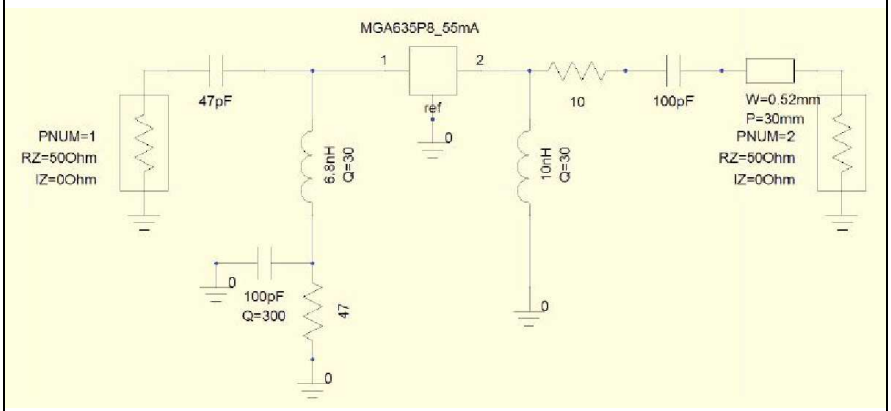

Fig 44: Using this simulation diagram the ANSOFT Designer SV is satisfied and delivers exact predictions.

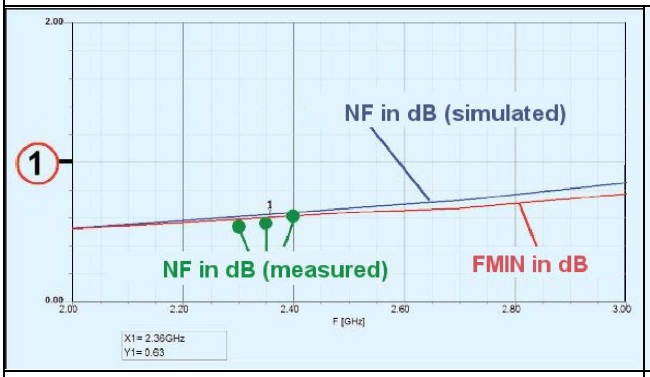

Fig 45: A noise figure of 0.64dB in the simulation, but measured only 0.6dB - that's fun!

Fig 46: S21 is practically identical to the measurement (approximately +17dB).

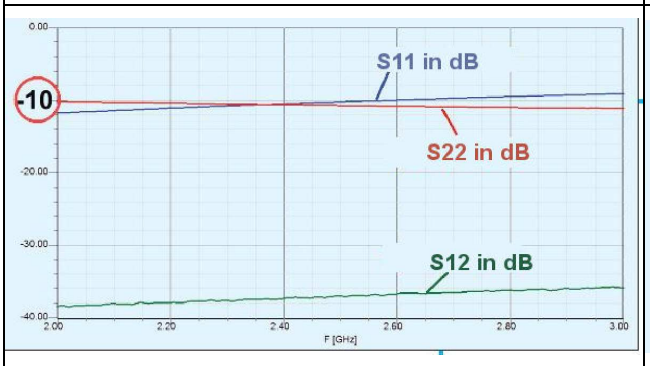

Fig 47: S11 and S22 are about -10dB in the intended frequency range, while S12 is well below -30dB.

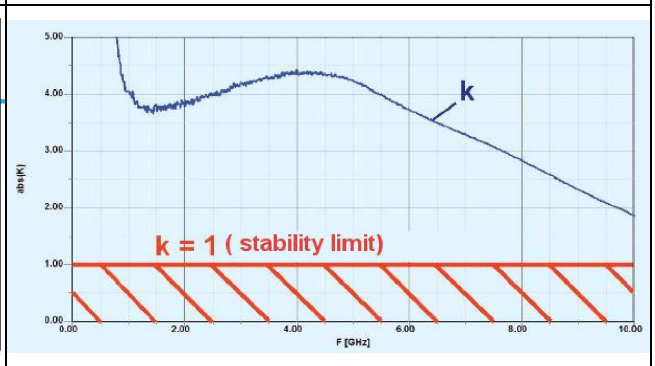

Fig 48: So you can imagine a "good stability".

9. The input bandpass filter for 2375MHz

9.1. Requirements and specification

The 13cm band is located between 2300 and 2450MHz with certain small restrictions depending on the region. Above 2450MHz is the WLAN range for PCs and Notebooks, which is why the passband of the bandpass filter was set as 2270 to 2480MHz with a centre frequency of 2375MHz.

It is designed as a microstrip version with coupled lines of Z = 50Ω and should have low passband attenuation combined with high stopband attenuation. For a filter order N = 3 the increase in the stopband attenuation with the frequency is still a bit poor and so N was increased to "5". Thus, the following requirement specification applies to the bandpass filter:

Chebyshev type		
Ripple	=	0.3dB
Filter order N	=	5
Bandwidth b	=	210MHz
Lower limit frequency f_{p1}	=	2.27GHz
Upper cutoff frequency f_{p2}	=	2.48GHz
Centre frequency f_0	=	2.375GHz

The most common PCB material "ROGERS R04350B" used today with the following data:

Substrate thickness h	=	0.76mm
Dielectric constant εr	=	3.66
Double-sided copper layer t	=	35µm
Surface roughness about		2µm
Loss factor tand	=	approximately 0.0031 at 2.5GHz

The board size is 30mm x 50mm and the housing used has a "cover height" = 13mm (= distance between the shield cover and the board).

9.2. Bandpass filter design with the ANSOFT Designer SV

9.2.1. The feedline with Z = 50Ω

First, the connections to the SMA socket for the input and output of the filter circuit are designed. It is fitted into a milled aluminium housing. Since the ANSOFT Designer integrates an excellent line calculator, you should use it and it works like this:

a You start the "Designer" and choose "Insert Circuit Design".

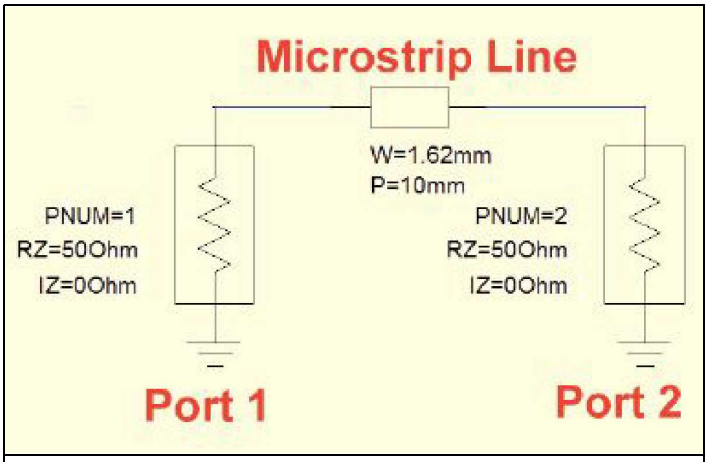

Fig 49: That's how easy it is to create a simple circuit with a 50Ω feedline between 2 ports ready for simulation.

b Now you build a simple circuit consisting of a microstrip line between two ports and click the right mouse button on the circuit symbol of the line (**Fig 49**).

c This opens the line calculator "TRL" where the above material data, the characteristic impedance of Z = 50Ω, electrical length and frequency f = 2.3GHz are entered (**Fig 50**). The program calculates the required line width = 1.62mm when "Synthesis" is clicked.

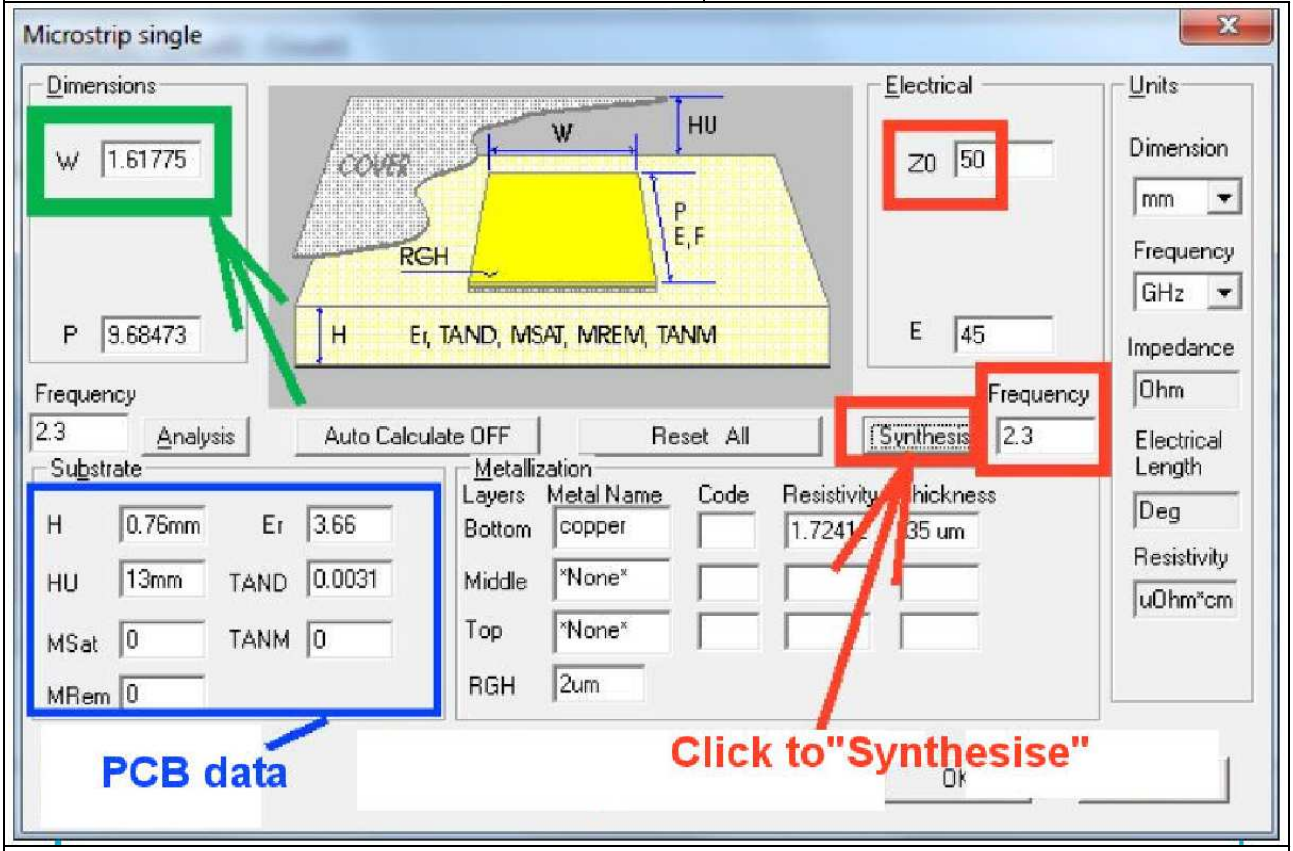

Fig 50: And then with a right-click on the fedline calls up the line calculator (see text).

Fig 51: This shows success and accuracy achieved with a line width of 1.62mm up to 10GHz

With that on the screen you should simulate the simple test circuit and look at the S11 curve up to 10GHz. As **Fig 51** shows there is no reason for criticism.

9.2.2. The filter development

Continue with "Insert Filter Design" (under "Projects") and choose the "Edge coupled Chebyshev Microstrip" version. Using this filter and material data shown above the basic design is produced quickly. It looks like this:

First and sixth line pair:

Length 19.5mm
Width 0.6545mm
Distance 0.4389mm

Second and fifth line pair:

Length 19.29mm
Width 0.7566mm
Distance 1.1mm

Third and fourth line pair:

Length 19.27mm
Width 0.7636mm
Distance 1,285mm

However, this is only the start of more work because you have to realise each coupled line in the circuit using the "MS Coupled Lines with Open Ends, Symmetric", in order to consider the "Open End Extension". In addition, microstrip steps are inserted between lines with different widths. Only four of them are needed here, because the four middle line pairs have the same width of 0.76mm. The feedline with a width of 1.62mm for Z = 50Ω should not be missed. Then the work really starts because by considering the "Open End Extension" AND the steps you get a shift of the filter curve towards low frequencies AND a deterioration of S11 and S21 - which you have to correct manually. This starts by changing the line length of the middle line pair with subsequent fine corrections of the other pairs until the desired reflection curve S11 is reached (because the S11 display is much more sensitive and informative than the S21 display!). Then by a simple change of all line lengths by the same factor.

"Simulation of the Measured Centre Frequency" / "Desired Centre Frequency"

will shift the pass band curve to the correct position. This creates the circuit diagram shown in **Fig 52** with the correct line lengths.

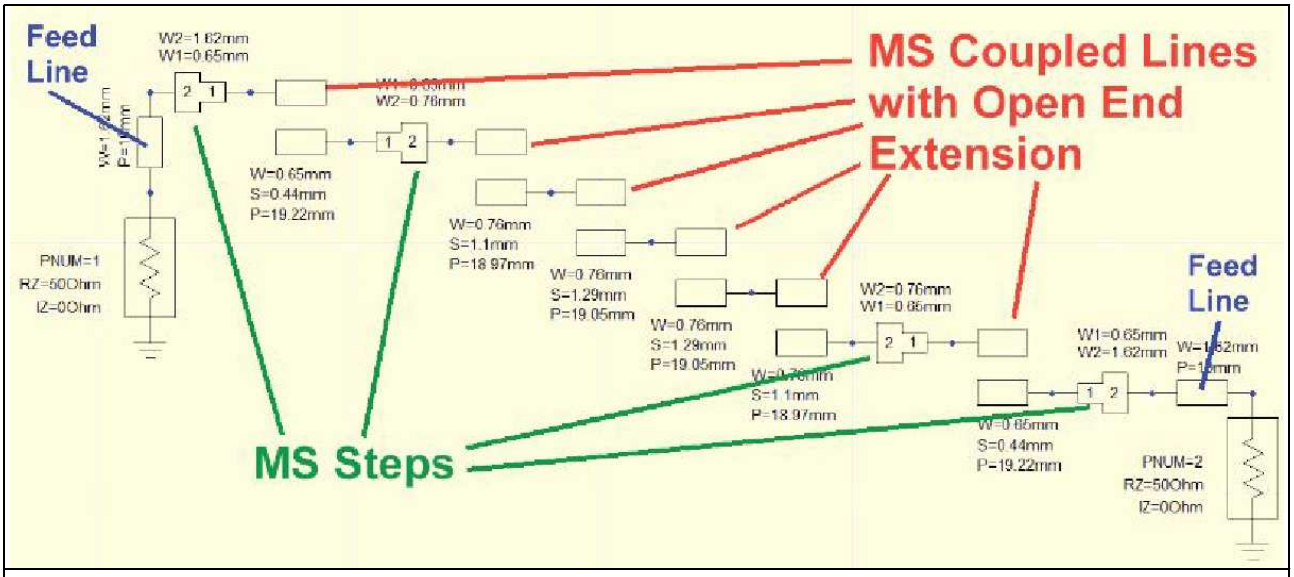

Fig 52: The final simulation circuit of the bandpass filter after all corrections (see text).

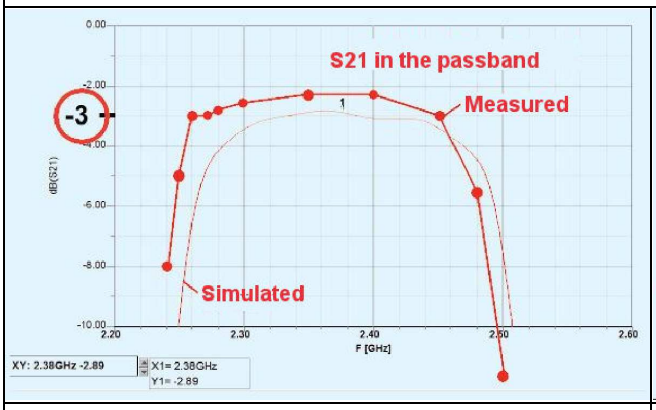

Fig 53: This is almost a dream come true: The simulation predicts an attenuation of something like 3dB in the passband; the measurement surprises with a minimum of 2.4dB

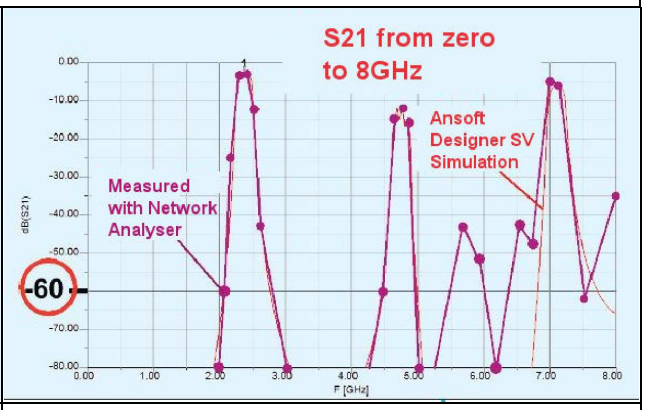

Fig 54: Theory and practice go together up to 8GHz.

Now the measurement results compare to the design.

S21 in the passband shown in **Fig 53** is a nice surprise. The attenuation is smaller than expected and lies well below 3dB at the centre frequency (f = 2.38GHz). The transmission curve could do with a slight frequency shift upwards of about 20MHz.

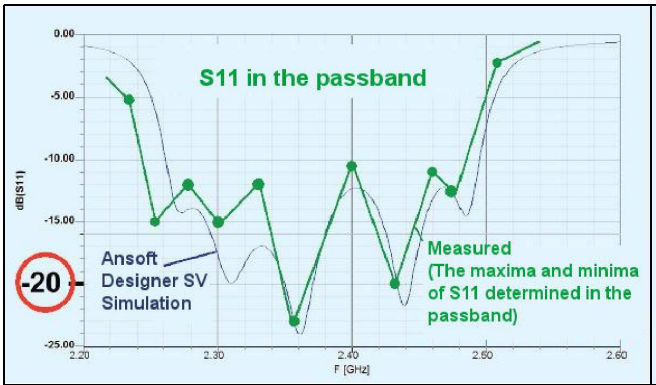

Fig 55: No major surprise with the reflection S11 were expected in the pass band. Only a slight upward shift of the measured curve is necessary.

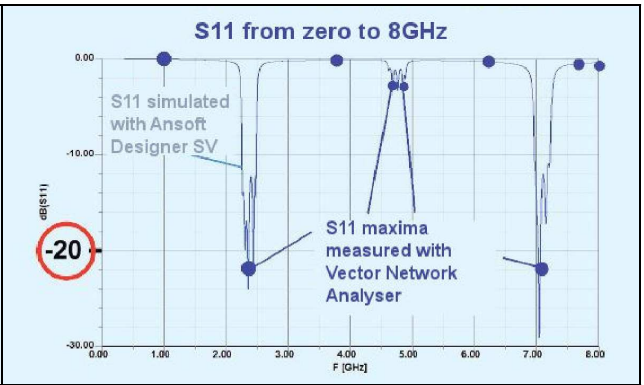

Fig 56: Even up to 8GHz S11 has nothing to complain about.

There are no surprises in the stopband up to 8GHz (**Fig 54**). Measurements are almost identical to the simulation. The dips are expected and predicted by theory.

There is little cause for criticism with the input reflection - neither in the passband (**Fig 55**) nor in the stopband up to 8GHz (**Fig 56**).

The layout was converted into a ROGERS R04350B board with a thickness of 0.76mm and dimensions of 30mm x 130mm. The printed lines are treated with "rub-on silvering". Conductive foam was glued to the inside of the lid to dampen housing resonances or waveguide effects at frequencies from about 6GHz. These cause deterioration of the stopband attenuation. **Fig 57** shows the reward for the effort with the filter in the housing used.

So this chapter has become an excellent testament to the quality of ANSOFT Designer SV.

Fig 57: The finished circuit in the milled aluminium housing. It is an impressive sight: size 30mm x 130mm.

10. The active broadband mixer ADL5801

10.1. Introduction

This is shown in **Fig 58.** This is not just a simple "Gilbert Cell" (active double balanced mixer), but a "complex machine" that works up to 6GHz because of the SiGe technology used.

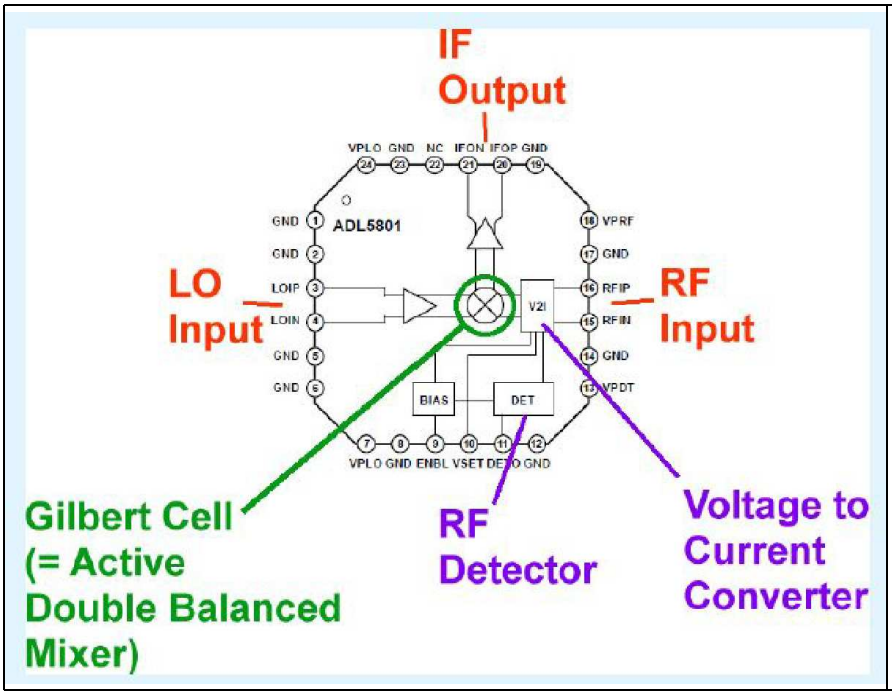

Fig 58: The active Double Balanced Mixer ADL5801 looks suspiciously normal, but there are some tricky extra details inside (see text).

There is an integrated amplifier at the LO input in order to cater for smaller oscillator levels. There is also a built in amplifier with a gain up to +7.8dB at the IF output. This compensates for the conversion loss.

The RF input is more sophisticated:

If required the RF signal amplitude can be monitored with a detector and at higher levels the quiescent current in the mixer is automatically increased. This increases the IP3 point resulting in significantly improved linearity. If the high input level falls the quiescent current is reduced. Not only does this benefit the power consumption, it also improves the "SSB noise figure"

10.2. The "Evaluation Board"

An evaluation board is available from ANALOG DEVICES for about $120. The details shown in **Fig 59** are not difficult to understand:

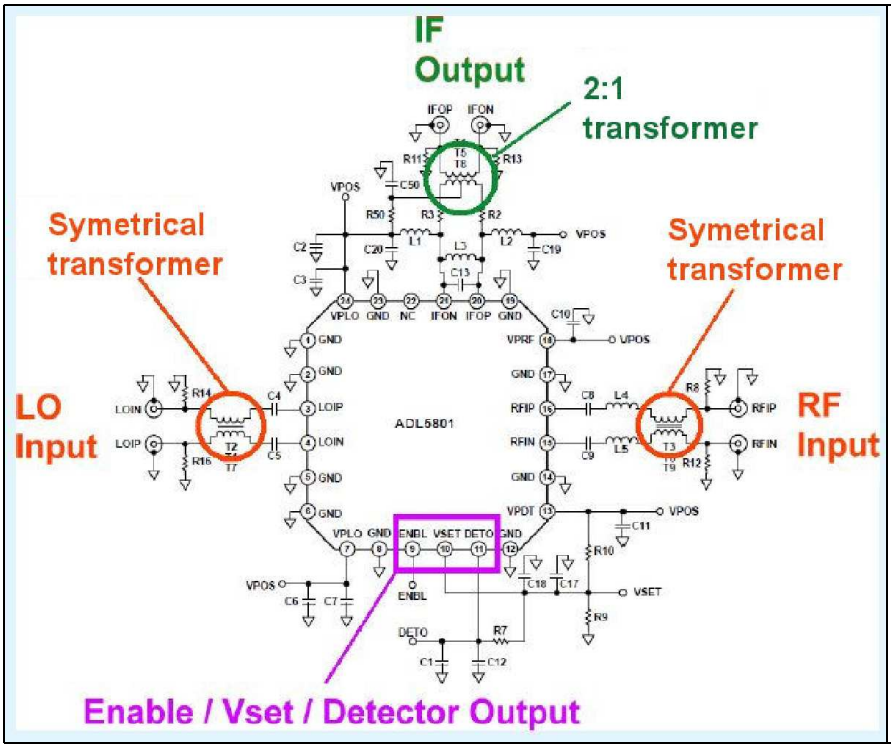

Fig 59: Of course you have to deal with these details separately when using this evaluation board (see text).

The LO input and the RF input use symmetrical transformers, while the IF output is 50Ω using a 2: 1 transformer.

For "normal" operation as a downconverter the "EVAL pin" is set to "HIGH" to turn off the automatic quiescent current increase in the mixer with strong input signals mentioned above. In addition R7 is removed that passes the detector output voltage to the BIAS circuit. The operating point setting is made by the control voltage "VSET". An additional resistor (R10 = 560Ω) has to be soldered onto the board connected the supply voltage. This gives a value of VSET = 3.8V, which is recommended in the data sheet for such a case and is used for many measurement curves that are listed. The device now has a quiescent current of 125 mA.

The total gain of the mixer is on average about zero dB (the conversion loss of a passive ring modulator would be more). The IP3 point is between + 17 and + 30dBm depending on the operating frequency and selected quiescent current.

11. The PLL conversion oscillator

This also comes as a finished "Evaluation Board" from ANALOG DEVICES using the lC

"ADF4351". This uses the latest technology and costs about $150. First, take a look at the "Functional Diagram" (**Fig 60**). The main sections are highlighted by blue frames. Together with the red connection lines the basic circuit of the PLL can be recognised:

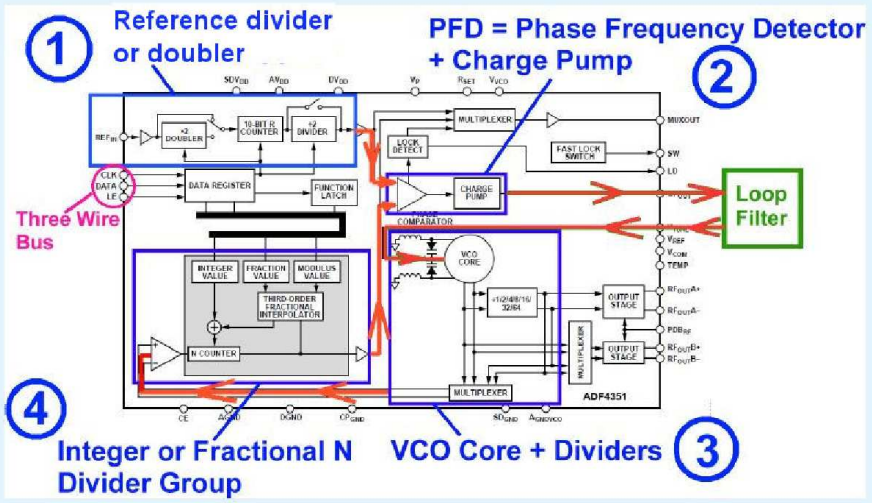

Fig 60: The ADF4351 is a modern PLL synthesiser with some extremely wild features (see text).

1 A programmable 10 bit divider can be used to lower the 25MHz crystal oscillator signal supplied to pin "REFIN". In addition doubling or halving is possible.

This is controlled using a 3-wire bus to give the the desired synthesiser output frequency.

2 The selected reference frequency feeds a PFD (Phase Frequency Detector) that is connected to a charge pump. This supplies the tuning voltage for the VCO but it needs to pass through the external loop filter first. This not only limits the capture, tuning and sustaining range but also stops the residual RF components of the free running the VCO.

3 The VCO operates over a frequency range from 2200MHz to 4400MHz. This is not achieved using a single circuit but is switched between three different VCOs. They provide the following frequency ranges (that overlap slightly):

Oscillator 1: 2200 to 2900MHz

Oscillator 2 2900 to 3700MHz

Oscillator 3: 3700 to 4400MHz

The "Oscillator Core" is followed by a switchable frequency divider (1/2/4/8/15/32/64) that feeds the output stage for output "A". Another output "B" provides access to the split VCO frequencies via a multiplexer. The divider is fed with the oscillator signal.

4 This part of the IC is the "wildest part" of the whole arrangement because it contains the “Know How”! It contains the hardware for integer division and fractional-N-division. It provides fractional division ratios and thus an (almost arbitrary) small step size of the tuning despite the quite high comparison frequency. So it avoids pure integer division giving small increments of settling and setting time (due to the high comparison frequency) and ensures small sideband noise.

However, all dividers and registers must be reset by the user for each frequency change! Just the thought of having to program all this in "C" for a microcontroller brings cold sweat to the forehead.

Therefore, ANALOG DEVICES has provided a free program "ADF435X Software" for easy operation via the PC screen and USB bus. This simplifies the matter and you don't need to worry about the signals that eventually close the PLL loop and feed the "Phase Frequency Detector". A small notebook with a USB port is sufficient to adjust the frequency.

The following example considers the details more closely.

The converter converts the centre frequency of the 13cm band (2375MHz) to 435MHz and requires an oscillator frequency of 1940MHz.

The ADF43SX software program is started, connection to the synthesiser evaluation board is made and the tab "Sweep and Hop" selected. An output frequency "A" of 1940MHz is set in "Frequency Hopping" In addition a frequency 100kHz higher is set in "B" i.e. 1940.1kHz to allow hopping to that frequency. The start button starts the "hopping process" and you only have to press the stop button at the right moment to get a constant output frequency of 1940MHz.

On the "Main Controls" window you will find all the registers involved and their required content. **Fig 61** shows this in more detail:

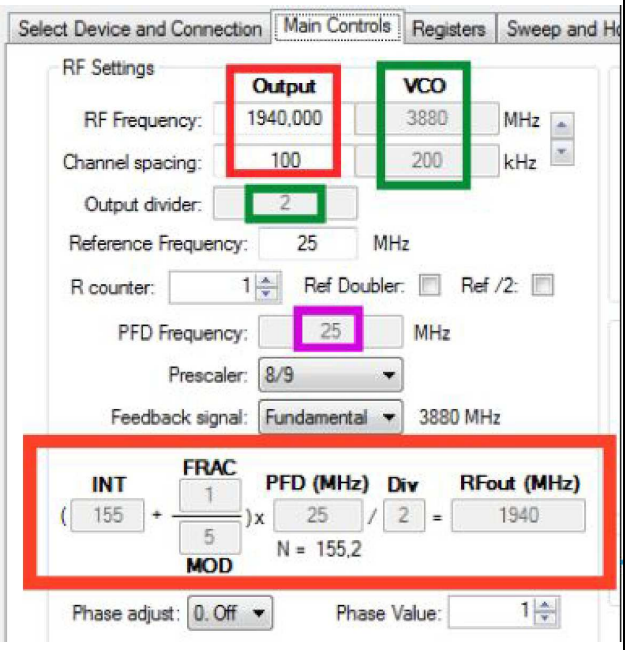

Fig 61: The software from Analog Devices shows exactly how the output frequency is generated (see text).

The current VCO frequency of 3880MHz is highlighted in green with a division by 2.

Pink indicates the PFD (Phase Frequency Detector) frequency. It is 25MHz and results in short setting and settling time.

Red shows the desired output frequency of 1940-MHz and the channel spacing of 100kHz and below the formula for determining the required division factor.

It uses the integer factor 155 and adds the fractional N factor "1/5"; therefore it is divided by 155.2. Multiplying this value by the 25MHz PFD frequency and dividing the total by 2 results in the desired output frequency of 1940MHz.

Now the process is repeated for the frequency "B" at 1940.1MHz. Only the fractional N-factor is changed to "26/125" giving the required 1940.1MHz.

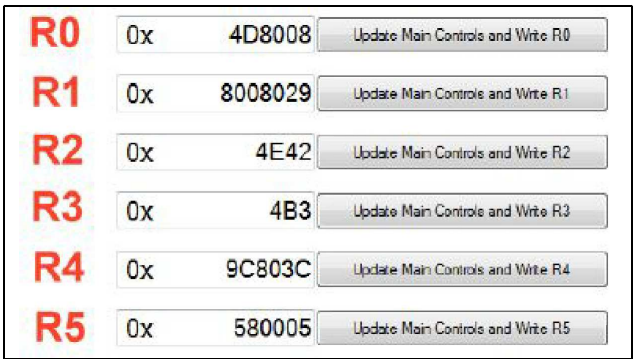

Fig 62: These are the registers to be written to set a particular frequency.

For information: The output level is between -4 and +5dBm, it can be programmed using register 4.

To round off this chapter and out of respect for the software programmer at ANALOG DEVICES, **Fig 62** shows the registers that must be written by the user for an output frequency of 1940MHz. These are 32 bit registers R0, Rl, R4 and R5 and 16 bit registers R2 and R3. A lot of sweat would be needed if you wanted to program this yourself using 8 or 16 bit microcontroller or "Raspberry

Pi". You always have to do the maths to determine both the integer divisor factor and the fractional N value. Fortunately, the actual tuning is only done via R0 / R1 / R2 and R4, the other registers control the many options that exist.

11.1. How does Fractional-N actually work?

As you can see, that's fine - using modified divisional relationships, but how do you do that?

The principle will be described by a simple example. Assume that the VCO initially is only followed by a divider with the division ratio of 100. An output pulse appears at the output whenever 100 VCO pulses are fed to the input and then the whole process begins again. This gives the VCO frequency divided by 100.

Fractional-N comes into play:

After this process the divider is switched to a divider ratio of "N + 1". So you get a pulse at the output when N = 100 + 1 = 101 VCO pulses have been fed to the input.

If this switching between "N" (here: N = 100) and "N + 1" (here N = 101) continues regularly, the divider output is a frequency modulated signal (in the rhythm of the switching) with a "centre frequency of exactly the VCO frequency divided by 100.5”

This can also be expressed as follows:

Output frequency = input frequency divided by (N + k)

The factor "k" (in this case: k = 0.5) should seem familiar, because that is what has been described above as the "fractional N-factor".

If we now change the "frequency of the divider switchover", we change this fractional N factor "k" between zero and one and have the answer to how it works.

The downside should not be overlooked: the output signal is now frequency modulated with a square wave voltage. The periodic frequency modulation produces a corresponding amount of spurious signals around the carrier in the output signal.

If the switching frequency is changed statistically, where only the mean value is important (use of a noise signal for divider conversion), the individual signals disappear, but a noise baseband is included in the output spectrum. Therefore many patents try to move this noise baseband or generate new spectral signals at higher frequencies so a lowpass filter can be used. But it is true: The IC manufacturers have done an incredible amount of good work and so that a signal-to-noise ratio of at least -90dBc is almost standard. And that is up to 10GHz!

So much extra effort is needed to find a reasonable compromise or a passable remedy for a good output spectrum. Accordingly the number of patents existing and publications is correspondingly large and the solutions sold in the ICs are usually complicated.

There are very nice and easy to understand introductions on the subject of "fractional-N" on The Internet. Especially the "Technical Brief SWRA029" from TEXAS INSTRUMENTS can be recommended as a starting booklet.

12. The oscillator lowpass filter with a cut off frequency of 2.1GHz

If the tuning range of the synthesiser ranges from 1865 to 2015MHz it is essential to use a filter (in this case a low pass filter at 2.1GHz) because there are still some secondary or harmonic frequencies

at the output of the oscillator. These would result in a forest of new spurious frequencies in the mixer.

This requires a very low and constant transmission loss up to 2015MHz, in order to keep the amplitude of the oscillator signal as constant as possible for the operation of the mixer. On the other hand, the attenuation should not only increase rapidly, but also achieve the highest possible value. This requires a high order filter to reduce the unwanted signals. The specification for a filter to fit the existing shielding housing looks like this:

Chebyshev lowpass		
Ripple	=	0.3dB
Filter order N	=	7
Cut off frequency	=	2.1GHz

Once again the design is done with the filter calculator from ANSOFT Designer SV and in **Fig 63** shows the circuit proposed. The capacitors are realised by (possibly square) microstrip line sections that are significantly wider than the 50Ω feedline. By contrast, the inductances are realised by extremely thin line sections (in comparison to the feedline).

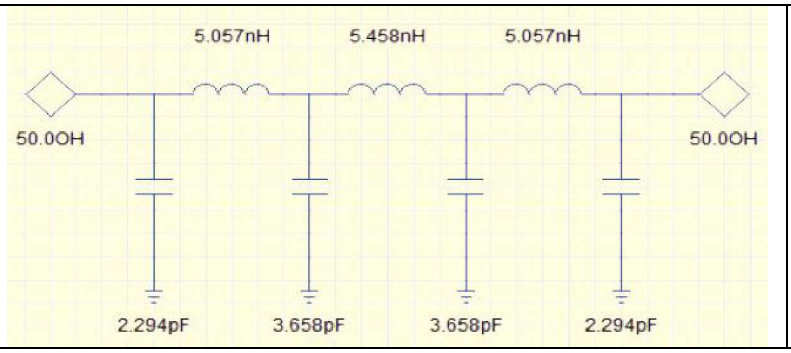

Fig 63: This image shows the ANSOFT Designer SV filter calculator after entering the requirements for the 2.1GHz lowpass filter.

For both components, the line lengths must remain well below one quarter of the wavelength – this means the electrical wavelength on the PCB. Otherwise the line properties are transformed and good stopband attenuation is lost. (For information: The data of a 50Ω line with an electrical length of 45 degrees on the existing PCB material of R04350B is: width = 1.62mm / length = 10.6mm).

The design procedure of the first 2.294pF capacitor starts with a very simple simulation. The capacitor is connected to a "Microwave Port" and a simulation shows S11 in the range of 2 to 2.5GHz (**Fig 64**). The result is displayed in the form of a Smith Chart. A marker is set at exactly 2.1GHz. It says: S11 = 1 / -113.07 degrees.

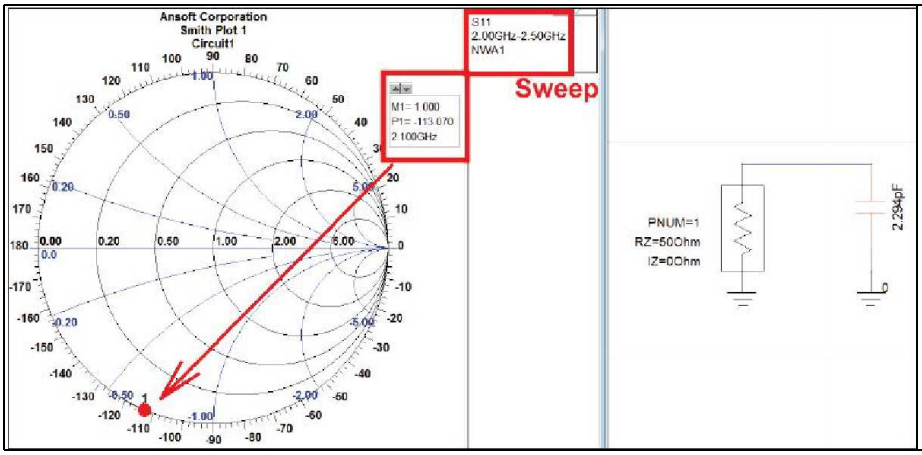

Fig 64: This is how you go about designing your capacitors. First the value of S11 for the real capacitor is simulated at 2.1GHz.

The capacitor is then replaced by an open square section of line 6mm wide and the simulation repeated. At a length of 6.78mm its S11 matches that of the real capacitor (**Fig 65**).

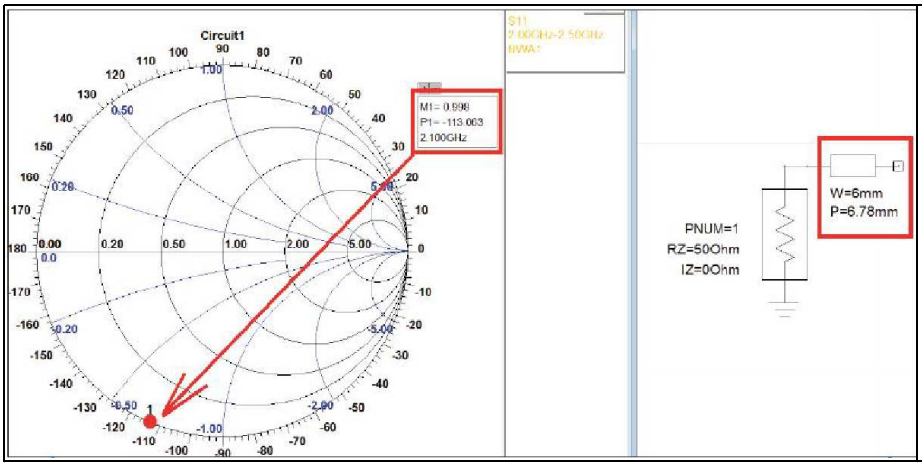

Fig 65: And then the real capacitor is replaced with a wide section of microstrip line with the same value of S11 (see text).

The procedure is then repeated for the second capacitor of 3.658pF. The line width should be increased, it is then, for example, 8mm x 8mm.

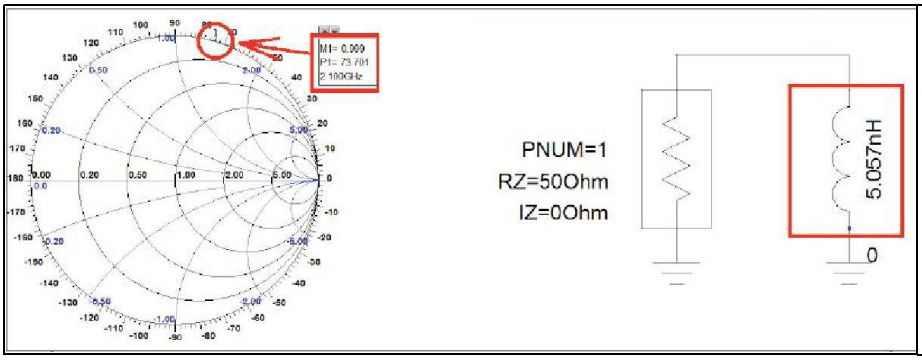

Fig 66: For the inductors we proceed in the same way: first determine S11 at 2.1GHz for a coil.

Continue with the inductors and take the same procedure for L1 = 5.057nH (**Fig 66**). This gives S11 = 1 / +73.7 degrees at 2100MHz. Subsequently, the inductance is replaced by a short circuited microstrip line with a width of 0.3mm. The length is varied until the same value for S11 is obtained, which is the case for L = 7.8mm (**Fig 67**).

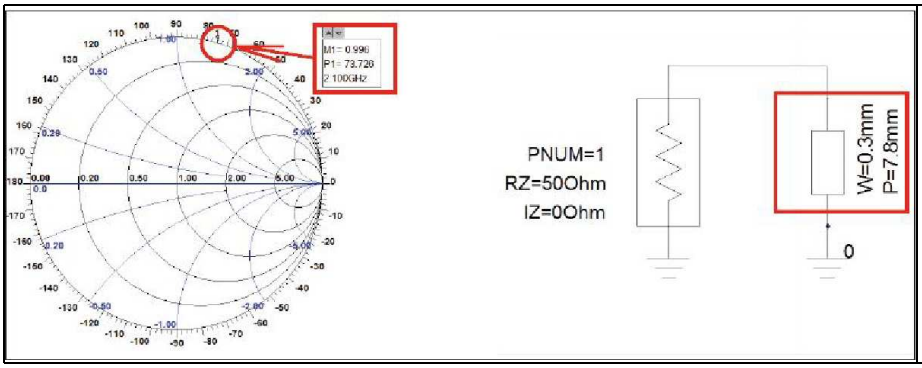

Fig 67: But then it has to be a very narrow piece of line if it is to become an inductor with the same S11 value.

Now the rest is only routine for L2 = 5.458nH, for this you need a length of 8.29mm at 8mm width.

So you can put together the complete simulation circuit. Do not forget to attach a feedline with Z = 50Ω (width = 1.62mm) to the left and right and to arrange "steps" between all line sections with different widths. The steps will shift the cut off frequency down and the ripple usually increases too. So you have to adapt the line sections again with laborious correction work. Finally the circuit shown in **Fig 68** should be achieved.

The comparison of simulation and measurement is interesting:

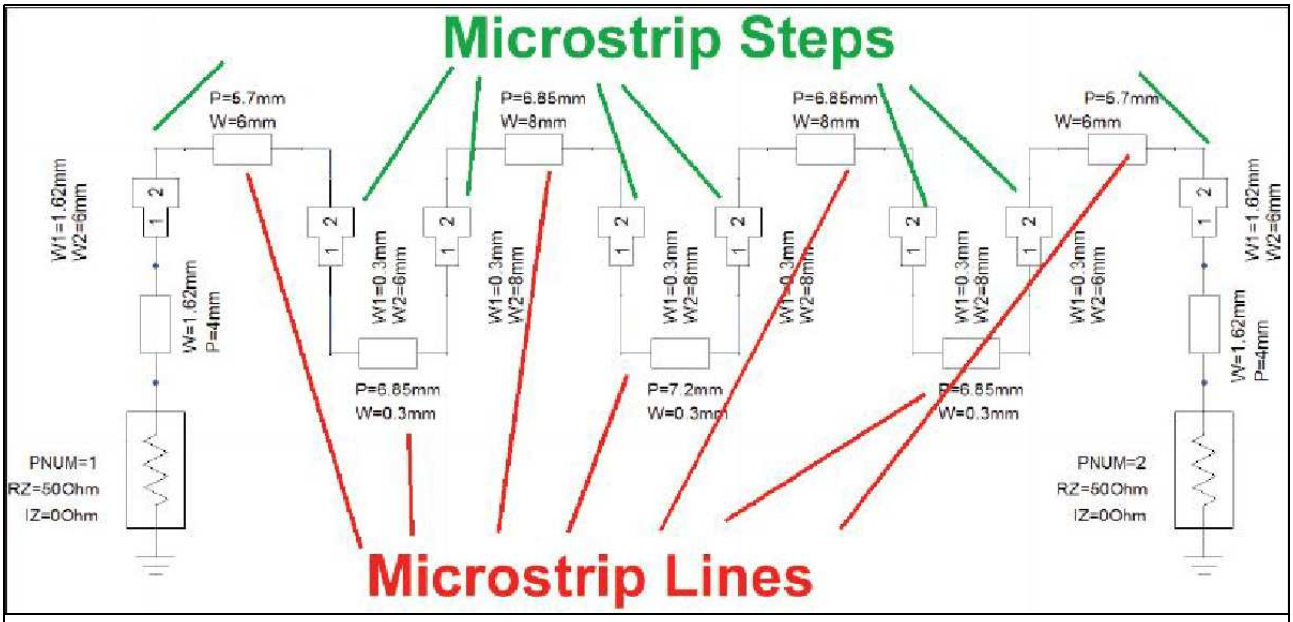

Fig 68: The simulation circuit requires some effort with the "Steps" until the required curve is achieved.

a The transmission loss in the passband (expressed by S21) is well below 1dB (**Fig 69**).

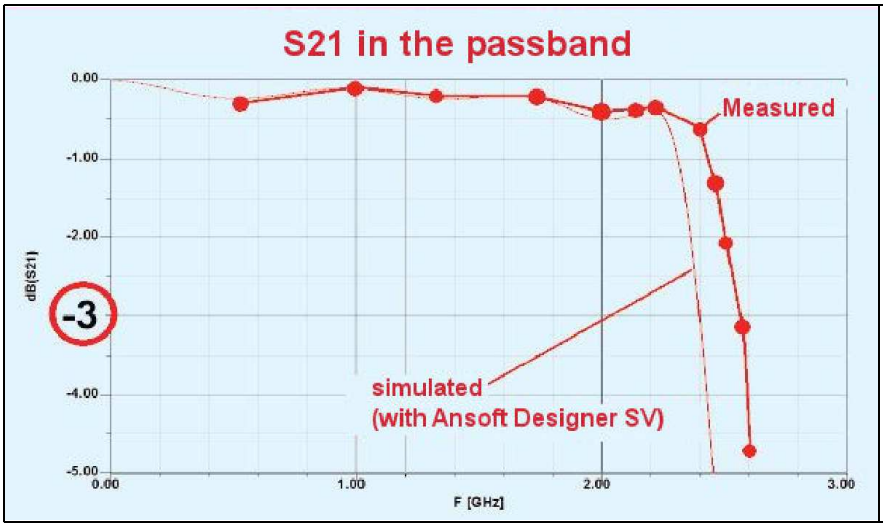

Fig 69: The reward for all the effort is an attenuation of less than 0.5dB in the range used by the PLL synthesiser

b Everything looks good in the stopband up to 6GHz with S21 an unexpected but welcome value as low as -80dB (**Fig. 70**).

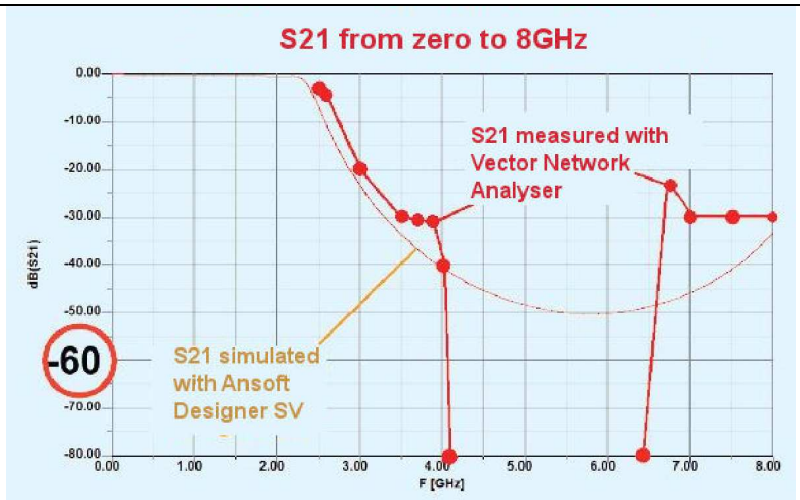

Fig 70: And the "hole" in the attenuation is acceptable.

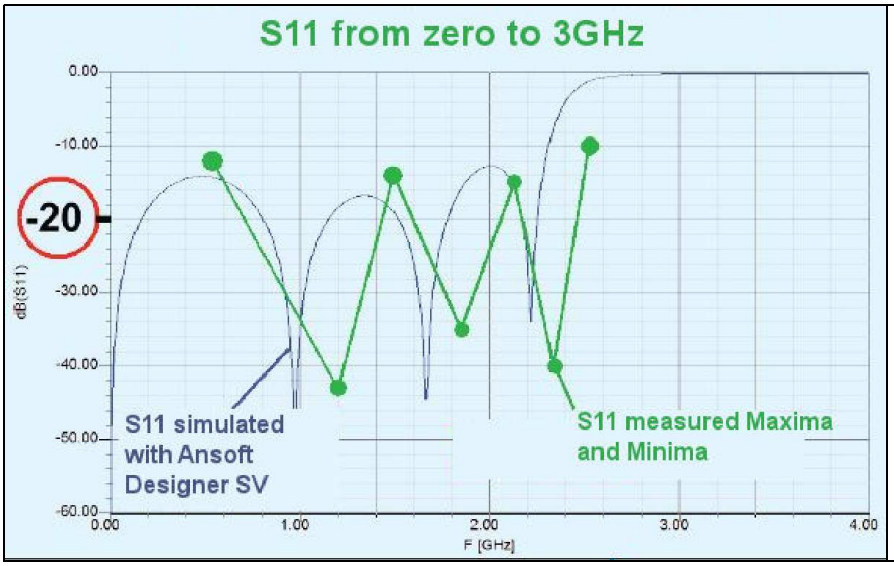

Fig 71: The S11 curve up to 8GHz clearly shows the slightly higher cutoff frequency of the passband compared to the simulation.

The S11 curve (**Fig 71**) shows a shift of the cut off frequency upwards by approximately 200MHz - this has already been indicated in the passband shown in **Fig 29.** But you can leave it that way!

The finished filter in its housing with the lid removed is shown in **Fig 72.** The lid is covered with damping material on the inside.

Fig 72: The finished module is pleasantly small with a board size of 30mm x 50mm.

13. The complete receiver and its behaviour

The finished experimental setup is shown in **Fig 73.** The two filters have been added around the converter and the mixer output is followed by the 435MHz bandpass filter. It feeds the calibrator block then it goes to the "RTL-SDR.COM" DVB-T stick. The output signal in the form of the USB IQ data stream is fed to a desktop PC and the small old notebook programs the PLL synthesiser.

Fig 74 shows the sensitivity measurement at 2375MHz. It shows a signal to noise ratio of 28dB for an input signal of -120dBm = 0.22µV, which is very pleasing.

The accuracy of the frequency tuning means that one can be completely satisfied! Finally, there are a lot of oscillators (signal generator / PLL conversion oscillator / DVB-T stick / program HDSDR, which is based on the clock oscillator of the PC) and their tolerances come into play so the conversion from 2375.000MHz is to 435.004MHz according to the screen display. The calibrator module was not even used.

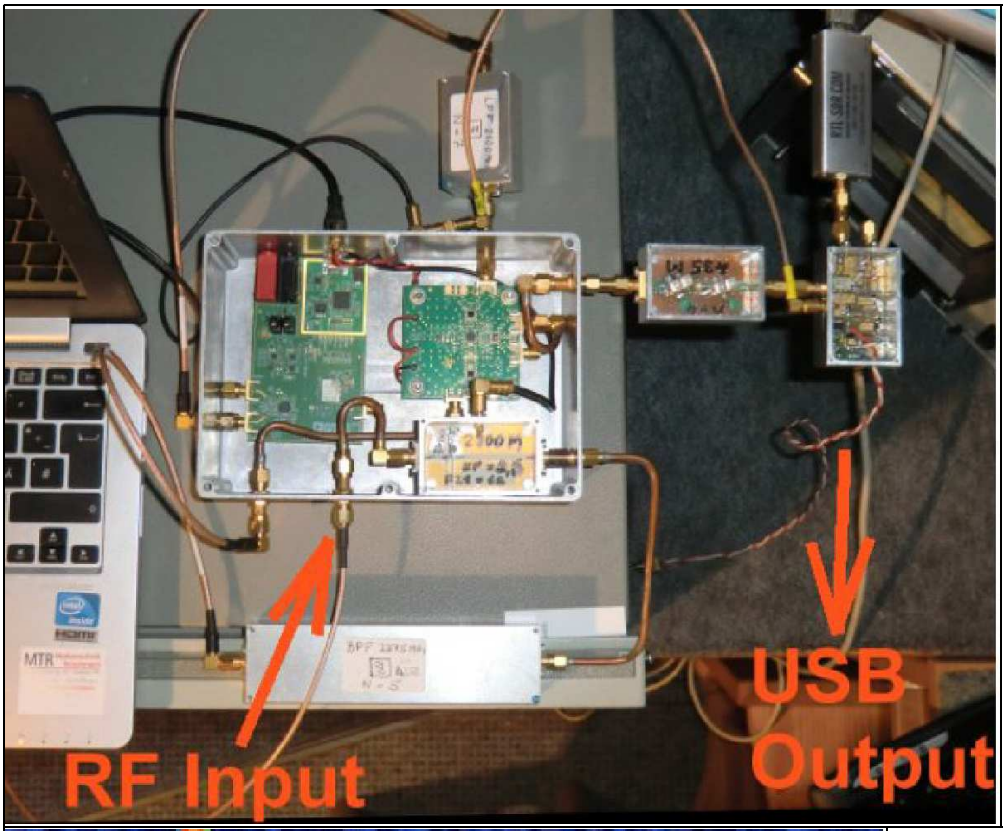

Fig 73: Of course, the complete arrangement needs some space in this form, but it could easily all be fitted into larger standard housing if required.

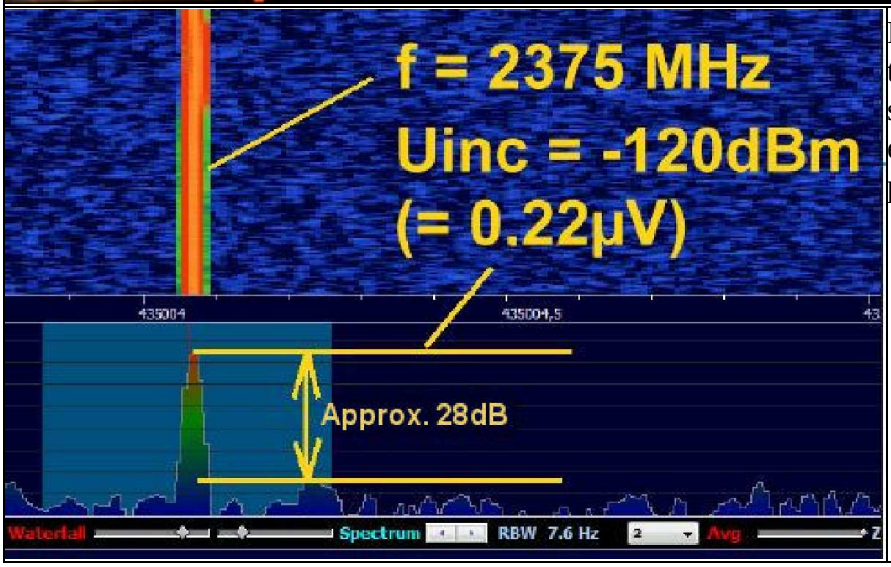

Fig 74: It took a long time but this receiver now has the same sensitivity as all previous projects using the gainblock principle.

14. References

Everything can be found on my homepage "www.gunthard-kraus.de" under the heading " Alle meine Veröffentlichungen in der Zeitschrift "UKW-Berichte" seit 1995”.

They are also in English on this web site. The current 4 part article is on the VHF Communication Magazine web site: www.vhfcomm.co.uk

The articles of interest are:

UKW Berichte issue 4-2012 and VHF Communications Magazine issue 2/2013: " Development of a preamplifier for 1 to 1.7GHz with a noise figure of 0.4dB"

UKW Berichte issue 2-2013 and VHF Communications Magazine issue 4/2013: “A low noise preamplifier for the 70cm band with a gain of 25dB and a noise figure of approximately 0.4dB "

UKW Berichte issue 4-2013 and on the VHF Communications Magazine web site: “A Low Noise Preamplifier With Improved Output Reflection For The 2m Band. First published in UKW Berichte 4/2013 "

UKW Berichte issue 1-2015: The HDSDR Program for Operating DVDB-T Sticks as Test Receivers and SDRs "

UKW Berichte issue 4-2016 and on the VHF Communications Magazine web site: “Receiver construction using 50 ohm modules (gain blocks) - Example Application: a low noise 2m receiver using a DVB-T stick. First published in UKW Berichte 4/2016 receiver "

UKW Berichte issue 1-2017 and on the VHF Communications Magazine web site: “Receiver building with Gainblocks. Example: 70 cm receiver "

UKW Berichte issue 2-2017 and on the VHF Communications Magazine web site: “Receiver building with gain blocks. Example: 23 cm receiver "