A Low Noise High Intercept Point Amplifier for 1850 to 1910 MHz PCS Applications using the ATF-331M4 Depletion Mode PHEMT

Application Note 1288

Introduction

The Agilent Technologies ATF-331M4 is one of a family of high dynamic range low noise PHEMT devices designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-331M4 is a 1600 micron gate width device available in the new subminiature leadless mini-pak package that measures only 1.2 mm by 1.4 mm. The device is performance tested at 2 GHz and has guaranteed RF performance at a V_{ce} of 4 V and I_d of 60 mA.

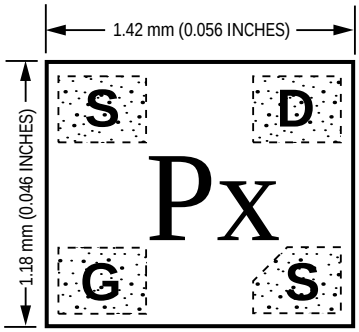
The small size and leadless feature offers the designer the ability to reduce circuit board layout size significantly. The top and bottom views of the M4 package are shown in Figure 1. The top side view includes a marking which indicates die type and date code. The bottom side metal contacts are shown only on the top view for orientation and are not visible from the top layer. The placement of the code also indicates the orientation of the four ports. The bottom-side metal contacts are gold plated nickel. A suggested printed circuit board layout etch pattern is shown in Figure 2. Hand soldering the ATF-331M4 is best accomplished by first applying a small amount of flux to the bottom of the part. Next step is to set the device in place on an already solder pre-tinned printed circuit board. For prototyping, a small 15 watt soldering iron can be used to reflow the solder around the mounting pads. In production, standard surface mount assembly techniques can be used to reflow the solder.

In this application note, the ATF-331M4 is described in a high dynamic range low noise amplifier designed specifically for PCS base station LNAs operating in the 1850 to 1910 MHz frequency range. When biased at a V_{ds} of 4 volts and an I_{ds} of 60 mA, the ATF-331M4 demonstration amplifier has a nominal 13.3 dB gain, a 0.8 dB noise figure and an output intercept point of +32 dBm. The amplifier has a nominal input return loss of greater than 20 dB and an output return loss of greater than 12 dB.

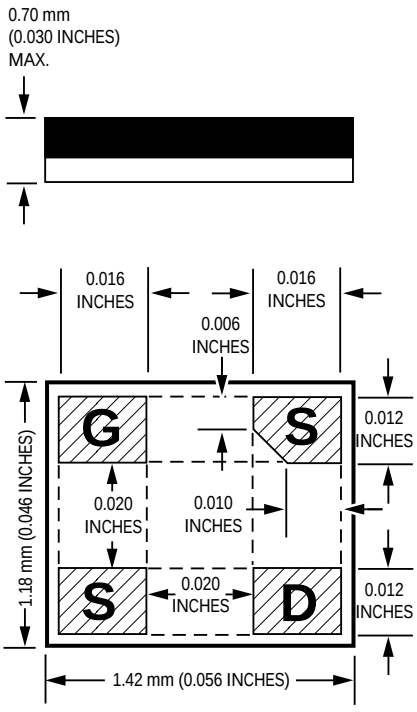
The design techniques presented in this application note can be applied to LNAs at other frequencies in the 900 MHz through 2500 MHz frequency range. The amplifier is etched on 0.031 inch thickness FR-4 printed circuit board material for low manufacturing costs. The amplifier makes use of low cost miniature multilayer chip inductors for small size.

Source Grounding of FETs and Biasing

One of the first items to consider in the design of any LNA is the method of biasing the device. Most microwave FETs are of the depletion mode type which re-



TOP VIEW OF 1.4 mm BY 1.2 mm MINI-PAK



BOTTOM VIEW OF 1.4 mm BY 1.2 mm MINI-PAK

Figure 1. Top and Bottom Views of the New Agilent Technologies Lead-less Mini-Pak Package

quires a negative voltage on the gate to pinch off the flow of drain current. Without the application of a negative voltage on the gate, the device will pull maximum drain current which is called I_{dss}.

The LNA described in this application note uses dc grounded source leads which necessitates the application of a negative voltage at the gate terminal to set the proper desired drain current. The negative voltage is required in addition to the positive voltage that is normally connected to the drain. This configuration is shown in Figure 3. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d, is dependent on the device's pinchoff voltage, V_p, and the saturated drain current, I_{dss}. I_d is calculated with the following equation:

$$V_{gs} = \left(V_p \left[1-\sqrt{(I_d/I_{dss})}\right]\right)$$

I_{dss} for the ATF-331M4 is specified at 237 mA typical. V_p is specified to be -0.5 V typical at 10% I_{dss} as opposed to I_d = 0 mA. Measuring V_{gs} in a high volume environment for I_d = 10% I_{dss} is easier than determining V_p when I_d = 0 mA . V_{gs} at 10% I_{dss} can be converted to V_p by substitution in the above formula. It was found that V_p = 1.462 x V_{gs} @ 10% I_{dss}. Therefore, V_p calculates to be -0.73 V. Substituting these parameters into the above equation predicts a typical V_{gs} for 60 mA I_d to be -0.36 V.

Each source lead is connected to ground through top side microstripline etch (LL) and a plated through hole to the bottom groundplane. The effect of these seemingly short lengths of transmission lines is in the form of additional inductance (LL) added in series with each source lead to ground. The additional inductance LL can have a very pronounced effect on amplifier performance. Its effect will be covered later in this application note.

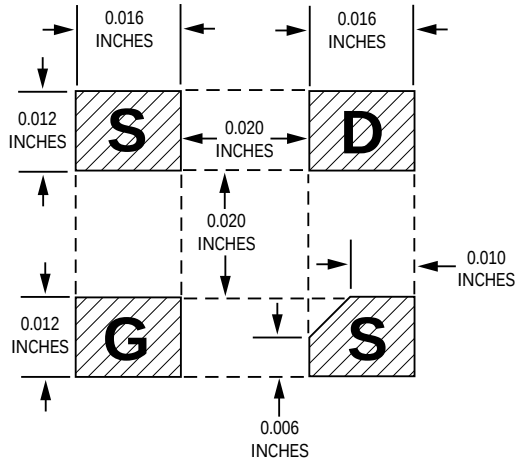


Figure 2. Suggested Printed Circuit Board Pad Layout for 1.2 mm by 1.4 mm Mini-Pak

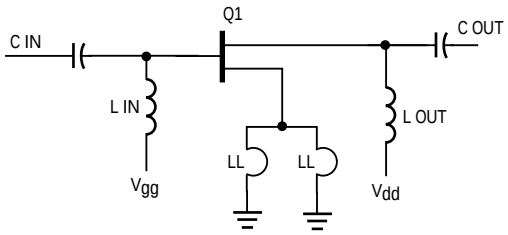


Figure 3. Biasing FET with DC Grounded Source Leads Necessitating Both Positive and Negative Voltage Power Supplies

Another option is to insert a resistor or resistors (Rs) in series with the source lead (s) to ground and dc ground the gate lead. This is shown in Figure 4. From a dc standpoint this has the same effect of making the gate more negative than the source, which is required to set the desired amount of drain current. From an RF standpoint, each of the source resistors must be bypassed to ground with a capacitor, Cs, which provides a low impedance at the frequency of operation. The capacitors are not perfect and therefore add additional series inductance with each lead. The additional inductance in series with each bypass capacitor is in addition to the inductance associated with the existing microstripline etch (LL) and plated through holes that provide the path(s) to the bottom ground plane.

As mentioned before, the inductance in series with each of the source leads has a pronounced effect on LNA operation. Some of the effects are undesired such as out-of-band gain peaking and stability issues. Other effects such as improved in-band stability and improved input return loss can be secured with a small or moderate amount of source inductance. Usually only a few tenths of a nanohenry of inductance is required. This is effectively

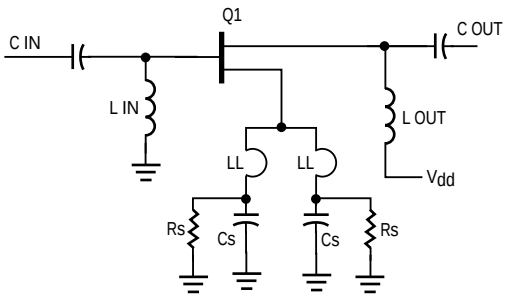


Figure 4. Biasing FET with Single Polarity Power Supply. Source Resistors are Used to Make Gate Voltage Negative with Respect to the Source.

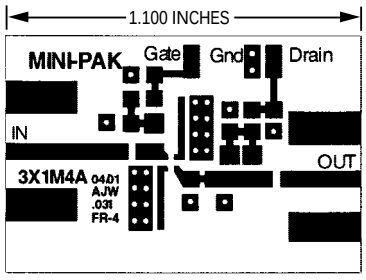


Figure 5. 1X Artwork for the ATF-3X1M4 Series of Low Noise PHEMT

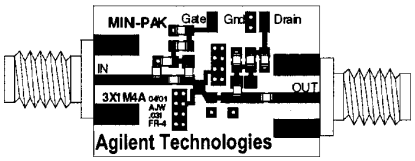


Figure 6. Component Placement Drawing for the ATF-331M4 Low Noise Amplifier

equivalent to increasing the source leads by only 0.050 inch or so.

The effect of using source inductance can be easily modeled using the Agilent Advanced Design System microwave circuit simulator. It is very important to properly model all circuit elements in order to accurately simulate circuit performance. The total effective source inductance in the simulation must include the source leads LL plus the associated lead inductance of the source bypass capacitors Cs and the effect of the plated through holes. It is therefore obvious that if source bypass capacitors are used in the design then the actual allowed source lead length LL will be less than if source bypass capacitors were not used.

The amount of source inductance that can be safely added depends on the device. Very short gate width devices such as the 200 micron gate width ATF-36163 can tolerate very little source inductance. Usually the inductance associated with just two plated through holes through 0.031 inch thickness printed circuit board is all that the device can tolerate. Hence the smaller gate width devices such as the ATF-36163 are typically used as low noise amplifiers for C and Ku Band applications such as TVRO and DBS. The usual side effect of excessive source inductance with short gate width devices is very high frequency gain peaking and resultant oscillations. The larger gate width devices such as the 1600 micron ATF-331M4 have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be.

LNA Matching Networks

The low noise amplifier is designed for a V_{ds} of 4 volts and an I_{ds} of 60 mA Typical power supply voltage, V_{dd}, would then be approximately 4.6 volts. The generic demo board shown in Figure 5 is etched on low cost 0.031" thickness FR-4 material. The demo board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal.

Extra length is included in this demo board to allow standard EF Johnson SMA connectors (part number 142-0701-881) to be used to prototype the amplifier. A completed demo board is shown in Figure 6.

The schematic diagram of the completed amplifier is shown in Figure 7. The amplifier is designed for DC grounded source leads which allows gain and output power to be adjusted by varying the gate voltage V_{gg}. The parts list is shown in Table 1.

The amplifier uses a high-pass impedance matching network for the noise match. The customary 2 element series C shunt L arrangement will match 50 ohms to just about any impedance on the smith chart as long as the elements are physically realizable. With the higher input impedances of some of the smaller 800 or 400 micron gate width devices, the simple 2 element matching network is usually matching 50 ohms to something in the hundreds or even thousands of ohms. The higher impedance transformation ratio also means lower values of series capacitance and lower values of shunt inductance. The 2 element high pass matching network also provides attenuation

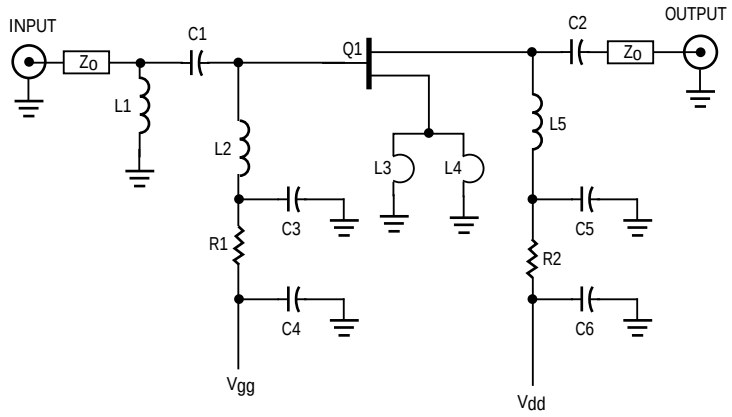


Figure 7. Schematic Diagram of the 1.9 GHz High Dynamic Lange Low Noise ATF-331M4 Amplifier

Table 1. Component Parts List for the ATF-331M4 Amplifier

C1	2.2 pF chip capacitor
C2	3.9 pF chip capacitor
C3, C5	8.2 pF chip capacitor
C4, C6	10,000 pF chip capacitor
L1	3.3 nH inductor (Toko LL1608-FH3N3S)
L2	5.6 nH inductor (Toko LL1608-FH5N6S)
L3, L4	Strap each source pad to the ground pad with 0.020" wide etch. The jumpered etch is placed a distance of 0.04" away from the point where each source lead contacts the source pad. Cut off unused source pad.
L5	15 nH inductor (Toko LL1608-FH15NK)
Q1	Agilent ATF-331M4 PHEMT
R1	50 Ω chip resistor
R2	10 Ω chip resistor
Zo	50 Ω Microstripline

below the cut-off frequency f_o of the network. The increased low frequency attenuation is quite often desirable to reduce amplifier gain below the normal frequency of operation. This characteristic may reduce the requirements placed on a front-end filter.

With the larger gate width of the ATF-331M4 and resultant lower input and output impedances, less impedance transformation is required in the matching networks. This generally means that the series capacitors are larger in value and the shunt inductors are also larger in value. The matching network tends to look more like a broad band bias decoupling network. The result is very little attenuation below the normal operating frequency. In addition to reduced out-of-band rejection, the amplifier circuit has a greater chance of being only conditionally stable as a result of increased low frequency gain.

The best solution is to add an additional element to one of the matching networks. Adding an additional shunt inductor to the input matching network will allow greater out-of-band rejection before the active device and is preferred. In the case of the ATRF-331M4 amplifier, a shunt inductor is added in parallel with the 50 ohm source impedance. The resultant PI network consists of two shunt inductors (L1 and L2) with a series capacitor (C1) in between. The 3 element network can then be optimized for best performance in-band while providing additional out-of-band gain reduction and improved amplifier stability down at 1 GHz.

L2 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C3. C1 also doubles as a dc block. The Q of L1 and L2 is extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608 inductor is a small multilayer chip inductor with a rated Q of greater than 40 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. The 3 element network has been optimized for both best noise figure coincident with very good input return loss. Resistor R1 and capacitor C4 provide low frequency stability by providing a resistive termination.

The amplifier uses a 2 element high-pass structure for the output impedance matching network. L5 and C2 provide the proper match for best output return loss and maximum gain. L5 also doubles as a means of inserting voltage to the drain. Resistor R2 and capacitor

C6 provide a low frequency resistive termination for the device which helps stability. C6 was chosen to be 10000 pF or 0.01 µF over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the F2-F1 difference component of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation.

Demonstration Board

The demonstration board is designed so that the designer has several circuit options with which to optimize performance for a particular application. Component mounting pads are provided near L5 to allow a resistor to be paralleled with L5 to lower gain and increase stability. A space is also provided for a resistor in series with the device drain lead. The space has already been jumpered on the demo board and can be easily removed with a sharp knife if a series resistance is desired. Neither of these resistors is required for this LNA design. It is important to remember that any amount of resistive loading in the drain circuit will effect gain and more importantly P1dB and OIP3.

The ATF-331M4 circuit design requires that an additional inductor, L1, be soldered to the input microstripline adjacent to C1. The other end of L1 is soldered to the same ground pad that C3 is soldered to.

Inductors L3 and L4 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demonstration board is designed such that the amount of source inductance can be made variable. The amount of inductance can be optimized during the prototyping stage and then fixed during production. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad would be connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the amplifier described in this application note, each source lead is connected to its corresponding ground pad at a distance of approximately 0.040" from the source lead. The 0.040" is measured from the edge of the source lead etch to the center of the ground strap. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. The subject of source inductance and its effect on amplifier performance is covered in Appendix I.

LNA Performance

The amplifier is tested at a V_{ds} of 4 volts and I_d of 60 mA. The measured gain and noise figure of the completed amplifier is shown in Figures 8 and 9. The gain measured a nominal 13.3 dB gain from 1850 to 1910 MHz. Noise figure measured between 0.7 and 0.8 dB over the same frequency range.

Measured input and output return loss is shown in Figure 10. The input return loss measured greater than 20 dB over the 1850 to 1910 MHz frequency range. The

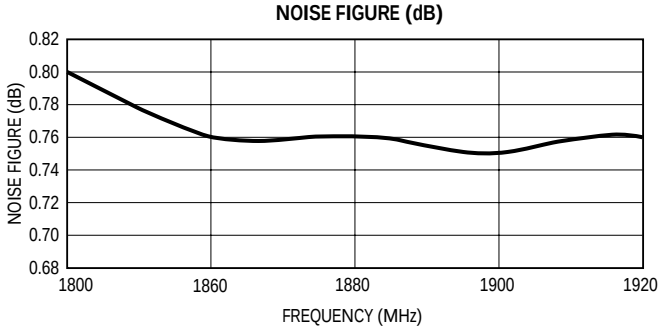


Figure 8. ATF-331M4 Amplifier Noise Figure vs. Frequency

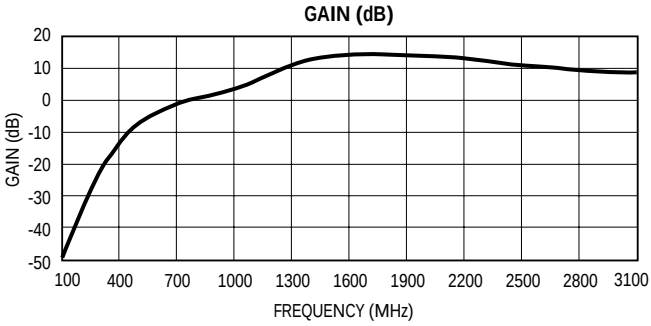


Figure 9. ATF-331M4 Amplifier Gain vs Frequency

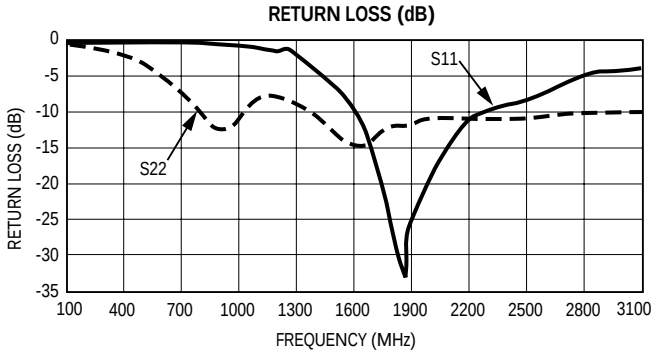


Figure 10. ATF-331M4 Amplifier Input Return Loss vs. Frequency

output return loss measured a nominal 12 dB in the 1850 to 1910 MHz frequency range.

The amplifier intercept point was measured using two test signals with a spacing of 1.25 MHz. The output intercept point (OIP3) was measured at 32.5 dBm at 1850 MHz and +33 dBm at 1910 MHz at a dc bias point of 4 volts V_{ds} and an I_d of 60 mA. Based on a nominal gain of 13.3 dB, the corresponding input intercept point (IIP3) calculates to be approximately +19 dBm.

ADS Simulation

The circuit was designed and optimized using Agilent's Advanced Design System. Figure 11 shows the circuit elements used in the input matching circuit. Figure 12 shows the circuit elements used in the output matching circuit. Figure 13 shows the ATF-331M4 device with its associated source grounding elements. The "MLIN" element is a convenient element for simulating the additional source lead length required to enhance stability. The "vias" represent the printed circuit board plated through holes. When self biasing the ATF-331M4, it is important to add the bypass capacitors to the source grounding circuit and any associated lead inductance. The results of the linear simulation are shown in Figures 14, 15, 16, and 17. Correlation between actual measured results and the simulation is very good.

Conclusion

The ATF-331M4 has been demonstrated in a low noise high intercept point LNA for PCS base station applications. The circuit provides less than a 0.8 dB noise figure with greater than 13 dB gain and greater than +32 dBm OIP3.

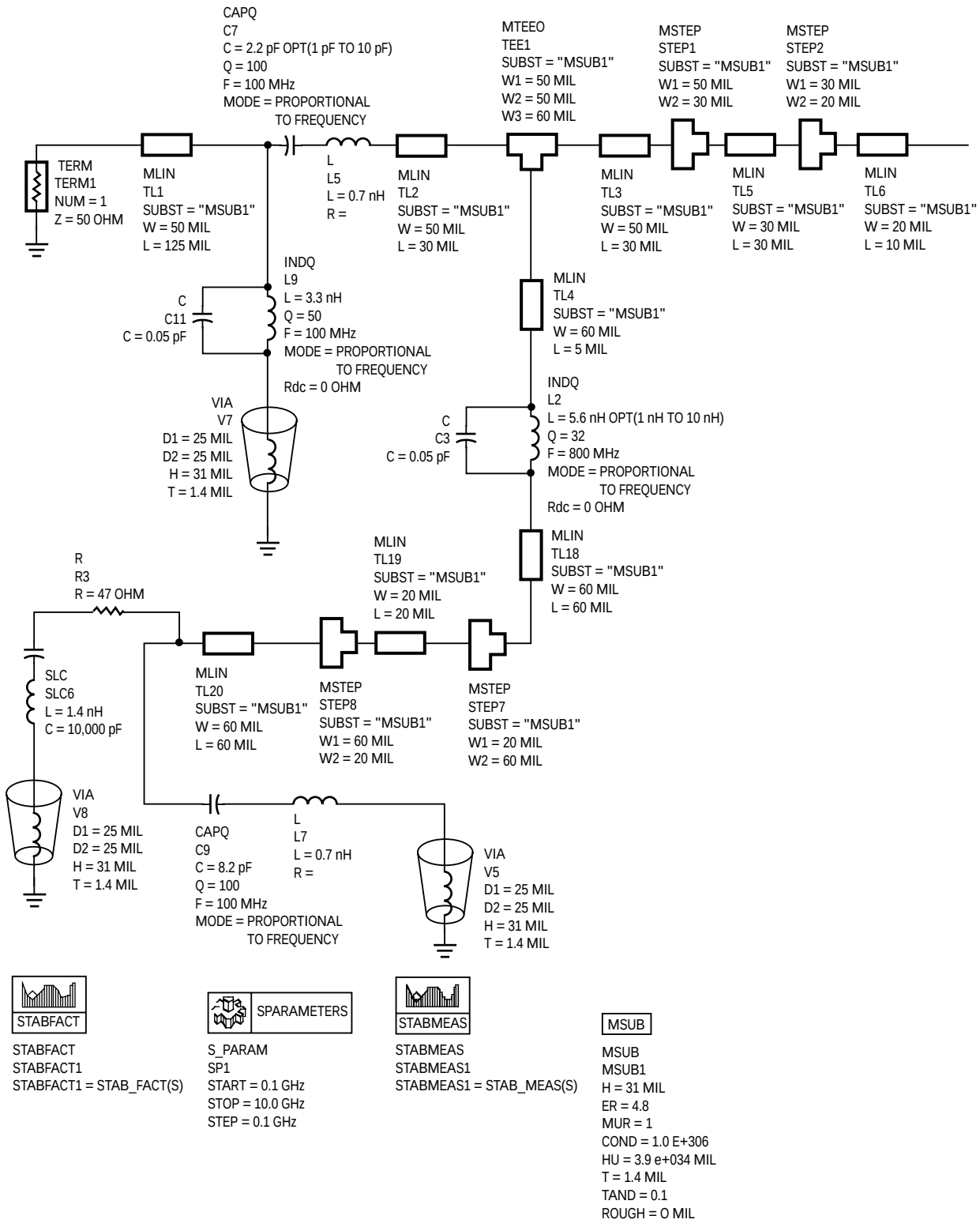


Figure 11. ADS Circuit File for Input Network for ATF-331M4 Low Noise Amplifier

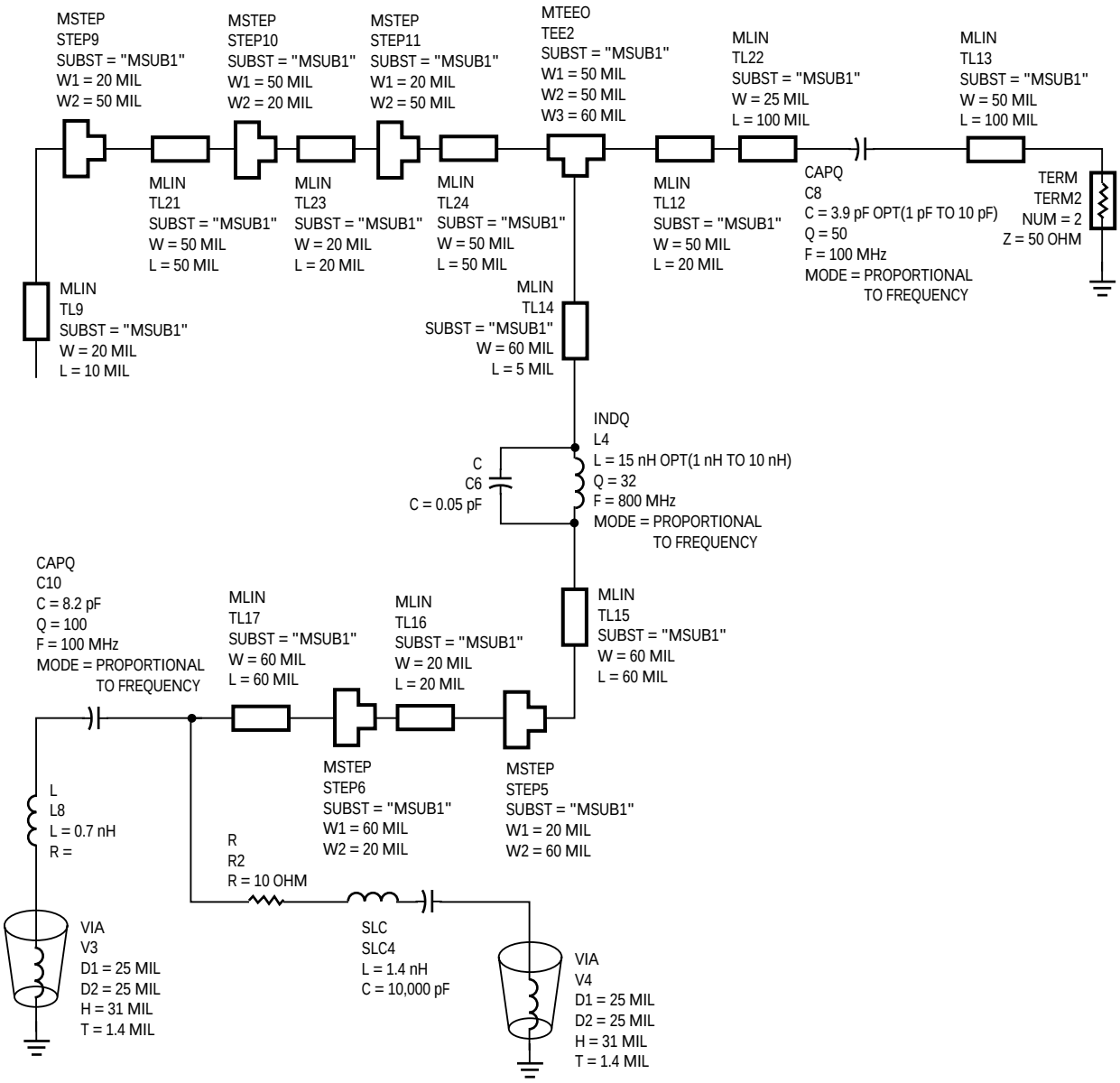


Figure 12. ADS Circuit File for Output Network for ATF-331M4 Low Noise Amplifier

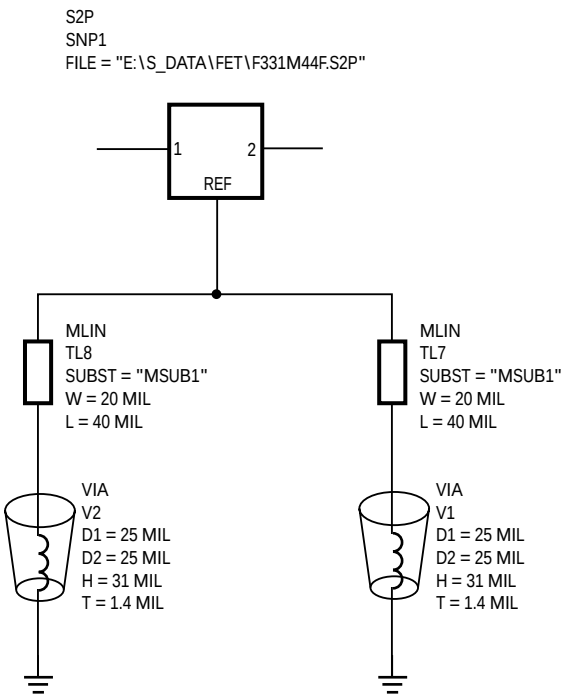


Figure 13. ADS Circuit File for ATF-331M4 and Associated Source Grounding Circuitry

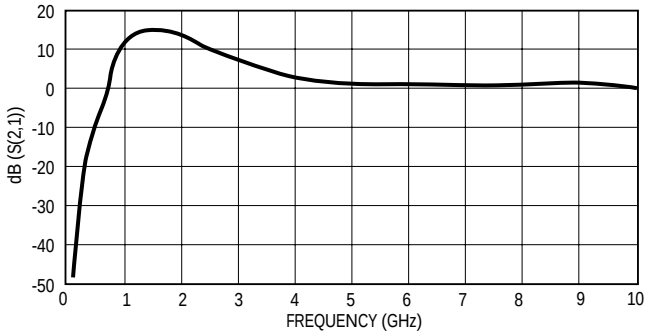


Figure 14. ADS Simulated S21 for ATF-331M4 Amplifier

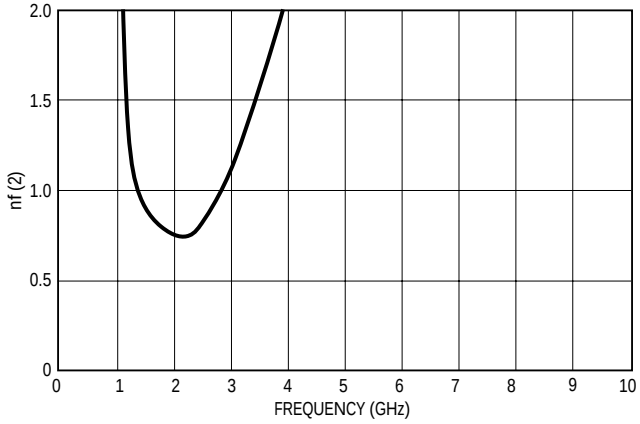


Figure 15. ADS Simulated Noise Figure for ATF-331M4 Amplifier

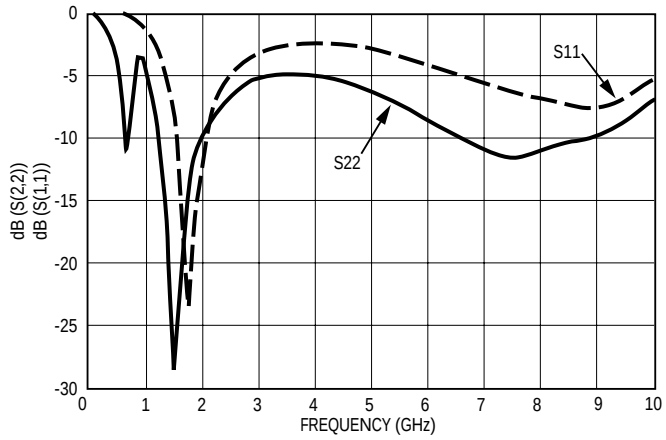


Figure 16. ADS Simulated S11 and S22 for ATF-331M4 Amplifier

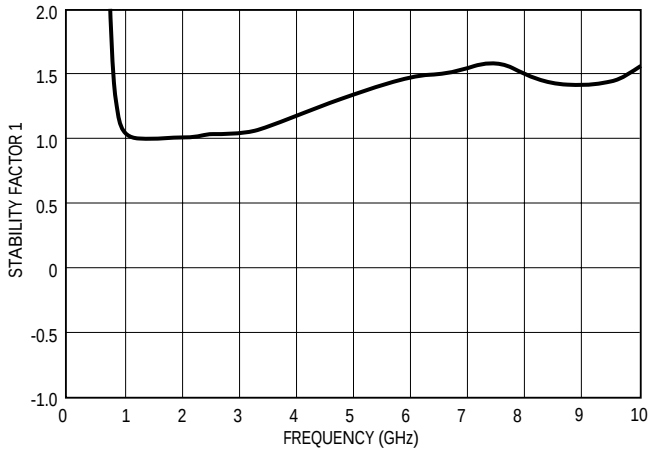


Figure 17. ADS Simulated Rollett Stability Factor K for ATF-331M4 Amplifier

Appendix I

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone to far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain rolloff will be gradual and smooth. Adding source inductance begins to add bumps or gain peaks to the once smooth gain roll-off. The source inductance while having a degenerative effect at low frequencies is having a regenerative effect at higher frequencies. This shows up as a very high frequency gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is fine as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

A wide-band plot of S21 for an amplifier using the 400 micron gate width ATF-35143 amplifier is shown in Figure 1. The ATF-35143 is used in this example because it is more sensitive to source inductance, i.e. high frequency gain is greater with smaller gate width devices. Similar behavior is to be expected using the 800 micron gate width ATF-34143 and the 1600 micron gate width ATF-331M4 but to a lesser degree

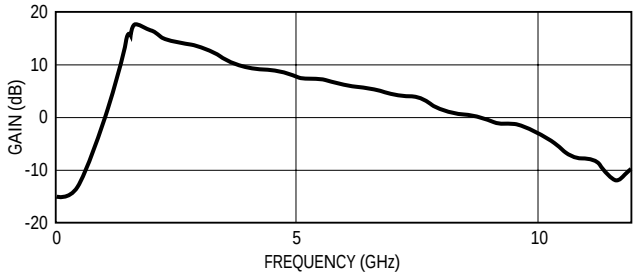


Figure 1. Wide-Band Gain Plot of Amplifier Using Minimal Source Inductance

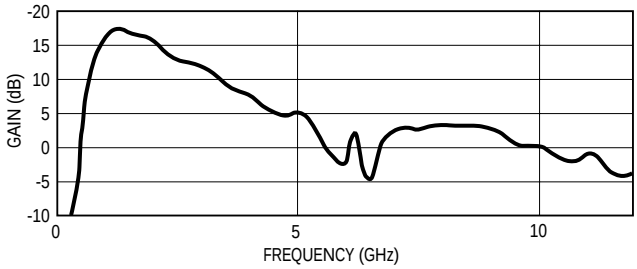


Figure 2. Wide-Band Gain Plot of Amplifier with an Acceptable Amount of Source Inductance

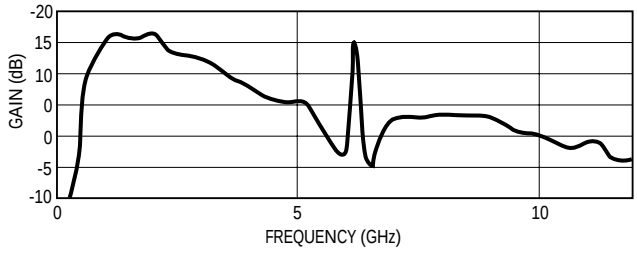


Figure 3. Wide-Band Gain Plot of Amplifier with an Unacceptable Amount of Source Inductance Producing Undesirable Gain Peaking

because of its greater gate width. The plot shown in Figure 1 represents an amplifier that uses minimal source inductance and has a relatively smooth gain roll-off at the higher frequencies.

The wideband gain plot shown in Figure 2 is for the same amplifier that uses additional source inductance. Increased source inductance improves low frequency stability by lowering gain. Input return loss will also be improved while noise figure will stay relatively constant. The effect of adding additional source inductance can be seen as some gain peaking in the 6 GHz frequency range. This level of gain peaking shown in Figure 2 is not considered a problem because of its relatively low level compared to the in-band gain.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak at about 6 GHz which could approach 20 to 30 dB. Its effect can be seen in Figure 3. The end result is poor amplifier stability especially when the amplifier is placed in a housing with walls and a cover. Larger gate width devices such as the 800 micron gate width ATF-34143 and the 1600 micron gate width ATF-331M4 will be less sensitive to source inductance than the smaller gate width devices and can therefore tolerate more source inductance before instabilities occur. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance.

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