

A Low Noise High Intercept Point Amplifier for 1930 to 1990 MHz using the ATF-33143 PHEMT

Application Note 1195

Introduction

The Agilent Technologies ATF-33143 is one of a family of high dynamic range, low noise PHEMT devices designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-33143 is the device with the largest gate periphery (1600 micron gate width) with 2 GHz performance tested and guaranteed at a V_{ce} of 4 V and I_d of 80 mA. The ATF-33143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

In this application note, the ATF-33143 is described in a high dynamic range low noise amplifier designed specifically for the 1930 to 1990 MHz PCS base station market. When biased at a V_{ds} of 4 volts and an I_{ds} of 80 mA, the ATF-33143 amplifier has a minimum of 13 dB gain, a 0.7 dB noise figure and an output intercept point of +32.5 dBm. The amplifier has an input return loss of 8 to 9 dB and an output return loss of greater than 20 dB.

The design techniques presented in this application note can be applied to LNAs at other frequencies in the 1500 MHz through 2500 MHz frequency range. The amplifier is etched on 0.031 inch thickness FR-4 printed circuit board material for low manufacturing costs. The amplifier makes use of low cost miniature multi-layer chip inductors for small size.

Source Grounding of FETs and Biasing

One of the first items to consider in the design of any LNA is the method of biasing the device. Most microwave FETs are of the depletion mode type, which requires a negative voltage on the gate to pinch off the flow of drain current. Without the application of a negative voltage on the gate, the device will pull maximum drain current which is called I_{dss} .

The LNA described in this application note uses dc grounded source leads, which necessitates the application of a negative voltage at the gate terminal to set the proper desired drain current. The negative voltage is required in addition to the positive voltage that is normally connected to the drain. This configuration is shown in Figure 1. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d , is dependent on the device's pinchoff voltage, V_p , and the saturated drain current, I_{dss} . I_d is calculated with the following equation.

$$V_{gs} = \left[V_p \left(1 - \text{SQRT} \left[\frac{I_d}{I_{dss}} \right] \right) \right]$$

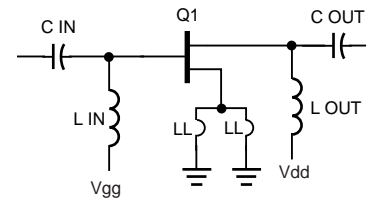


Figure 1. Biasing FET with dc grounded source leads necessitating both positive and negative voltage power supplies.

I_{dss} for the ATF-33143 is specified at 237 mA typical. V_p is specified to be -0.5 V typical at 10% I_{dss} as opposed to $I_d = 0$ mA. Measuring V_{gs} in a high volume environment for $I_d = 10\% I_{dss}$ is easier than determining V_p when $I_d = 0$ mA. V_{gs} at 10% I_{dss} can be converted to V_p by substitution in the above formula. It was found that $V_p = 1.462 \times V_{gs} @ 10\% I_{dss}$. Therefore, V_p calculates to be -0.73 V. Substituting these parameters into the above equation predicts a typical V_{gs} for 80 mA I_d to be -0.31 V.

Each source lead is connected to ground through top side microstripline etch (LL) and a plated through hole to the bottom groundplane. The effect of these seemingly short lengths of transmission lines is in the form of additional inductance (LL) added in series with each source lead to ground. The additional inductance LL can have a very pronounced effect on amplifier performance. Its effect will be covered later in this application note.



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Another option is to insert a resistor or resistors (R_s) in series with the source lead(s) to ground and then dc ground the gate lead. This is shown in Figure 2. From a dc standpoint this has the same effect of making the gate more negative than the source, which is required to set the desired amount of drain current. From an RF standpoint, each of the source resistors must be bypassed to ground with a capacitor, C_s , which provides a low impedance at the frequency of operation. The capacitors are not perfect and therefore add additional series inductance with each lead. The additional inductance in series with each bypass capacitor is in addition to the inductance associated with the existing microstripline etch (LL) and plated through holes that provide the path(s) to the bottom ground plane.

As mentioned previously, the inductance in series with each of the source leads has a pronounced effect on LNA operation. Some of the effects are undesired, such as out-of-band gain peaking and stability issues. Other effects, such as improved in-band stability and improved input return loss, can be secured with a small or moderate amount of source inductance. Usually only a few

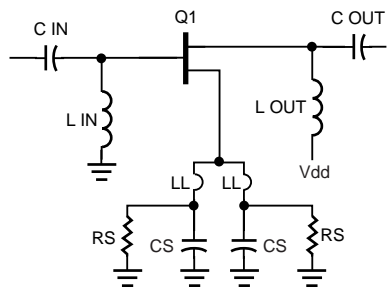


Figure 2. Biasing FET with single polarity power supply. Source resistors are used to make gate voltage negative with respect to the source.

tenths of a nanohenry of inductance is required. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily modeled using one of the Agilent/EEsof microwave circuit simulators. The amount of source inductance that can be safely added depends on the device. Very short gate width devices such as the 200 micron gate width ATF-36163 can tolerate very little source inductance. Usually the inductance associated with just two plated through holes through 0.031 inch thickness printed circuit board is all that the device can tolerate. Hence the smaller gate width devices such as the ATF-36163 are typically used as low noise amplifiers for C and Ku Band applications such as TVRO and DBS. The usual side effect of excessive source inductance with short gate width devices is very high frequency gain peaking and resultant oscillations. The larger gate width devices such as the 1600 micron ATF-33143 have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be.

LNA Matching Networks

The low noise amplifier is designed for a V_{ds} of 4 volts and an I_{ds} of 80 mA. Typical power supply voltage, V_{dd} , would then be approximately 5 volts. The generic demo board shown in Figure 3 is etched on low cost 0.031" thickness FR-4 material. The demo board offers the designer several biasing and circuit topology options during the prototyping stage. The demo board was designed such that the input and output impedance matching networks can be either

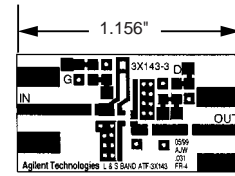


Figure 3. 1X artwork for the ATF-3X143 series of low noise PHEMT devices.

lumped element networks or etched microstrip networks for lower cost. Either low pass or high pass structures can be generated based on system requirements. The demo board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal. Extra length is included in this demo board to allow standard EF Johnson SMA connectors to be used to prototype the amplifier.

The schematic diagram of the completed amplifier is shown in Figure 4. The amplifier is designed for DC grounded source leads which allows gain and output power to be adjusted by varying the gate voltage V_{gg} . The parts list is shown in Table 1. The demo board as modified per this application note is shown in Figure 5. The modifications are discussed in the next section.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C_1) and a shunt inductor (L_1). The high-pass topology is especially well suited for PCS and WLAN applications as it offers good low frequency gain reduction which can minimize the amplifier's susceptibility to cellular and pager transmitter overload. L_1 also doubles as a means of inserting gate voltage

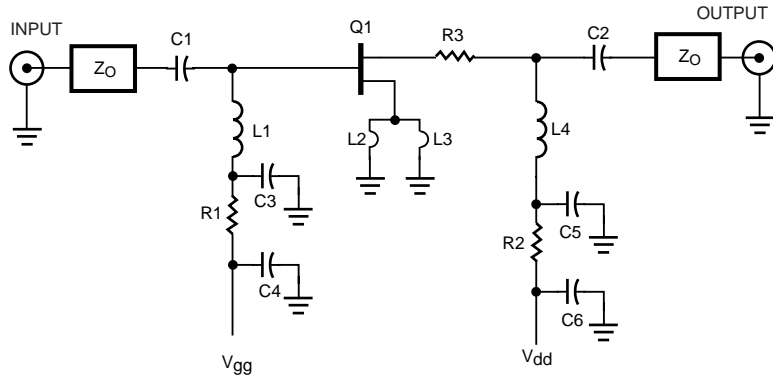


Figure 4. Schematic diagram of the 1.9 GHz high dynamic range, low noise ATF-33143 Amplifier.

Table 1. Component Parts List for the ATF-33143 Amplifier.

C1, C2	2.7 pF chip capacitor
C3	4.7 pF chip capacitor
C4, C6	10,000 pF chip capacitor
C5	10 pF chip capacitor
L1	10 nH inductor (Toko LL1608-FH10NK)
L2, L3	Strap each source pad to the ground pad with 0.040" wide etch. The jumpered etch is placed a distance of either 0.050" or 0.075" away from the point where each source lead contacts the source pad. Cut off unused source pad. See text for differences in performance.
L4	22 nH inductor (Toko LL1608-FH22NK)
Q1	Agilent Technologies ATF-33143 PHEMT
R1	50 Ω chip resistor
R2	10 Ω chip resistor
R3	Normally not used. Jumper with etch. See text for more information.
Zo	50 Ω Microstripline

for biasing up the PHEMT. This requires a good bypass capacitor in the form of C3. C1 also doubles as a dc block. The Q of L1 is extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-FH10NK is a small multilayer chip inductor with a rated Q of 45 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with

secondary emphasis on input return loss. Resistor R1 and capacitor C4 provide low frequency stability by providing a resistive termination.

The amplifier uses a similar high-pass structure for the output impedance matching network. L4 and C2 provide the proper match for best output return loss and maximum gain. L4 also doubles as a means of inserting voltage to the drain. Resistor R2 and capacitor C6 provide a low frequency resistive termination for the de-

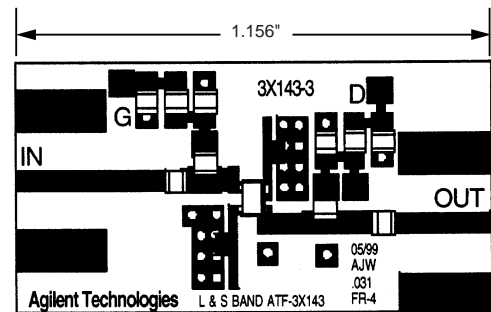


Figure 5. Component placement drawing for the ATF-33143 Low Noise Amplifier.

vice which helps stability. C6 was chosen to be 10000 pF or 0.01 μ F over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the F2-F1 difference component of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation. Resistor R3 was not incorporated in the original design as the circuit was unconditionally stable without R3. Depending on the final layout and component parasitics, circuit stability may be different. A small value of resistance in the 5 Ω to 22 Ω can be inserted at R3 to further help circuit stability. The use of R3 will lower gain and lower power output capabilities of the amplifier, so caution is advised.

The original demo board incorporates an additional series microstripline in the input impedance matching network. The microstripline is not required for this amplifier design and can be removed from the demo board. It should be replaced with a small 0.040" wide piece of etch. There is also space allocated for a resistor in series with the drain of the device. When R3 is not used, the gap should be bridged with a small piece of etch.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the 1900 MHz amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.050" from the source lead. The 0.050" is measured from the edge of the source lead to the closest edge of the ground strap. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. The subject of source inductance

and its effect on amplifier performance is covered in Appendix 1.

LNA Performance

The amplifier is tested at a V_{ds} of 4 volts and I_d of 80 mA. The source lead length is also varied to analyze its effect on LNA performance. The measured gain and noise figure of the completed amplifier is shown in Figures 6 and 7. The gain at 1960 MHz with $LL = 0.050"$ is a nominal 13.8 dB and 13 dB with $LL = 0.075"$. Noise figure at 1960 MHz is a nominal 0.69 dB with $LL = 0.075"$ and 0.73 dB at $LL = 0.050"$.

Measured input and output return loss is shown in Figures 8 and 9. The nominal input return loss at 1960 MHz is -7.3 dB with $LL = 0.050"$ and -8.6 dB with $LL = 0.075"$. Further improvement in input return loss is possible with some degradation in noise figure by altering the input impedance matching network. Increasing the amount of source inductance LL will offer further improvement in input return loss at the expense of in-band gain. Another potential problem may be out-of-band gain peaking as discussed earlier.

The output return loss measured -19 dB with $LL = 0.050"$ and -23 dB with $LL = 0.075"$.

The amplifier intercept point was measured using two test signals with a spacing of 1.25 MHz. The output intercept point (OIP3) was measured at a nominal +32.5 dBm at 1960 MHz at a dc bias point of 4 volts V_{ds} and an I_d of 80 mA. Based on a nominal gain of 13 dB, the corresponding input intercept point (IIP3) calculates to be nearly +20 dBm.

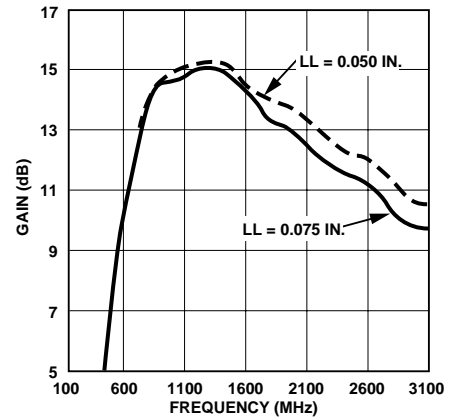


Figure 6. ATF-33143 Amplifier Gain vs. Frequency and Source Lead Length LL .

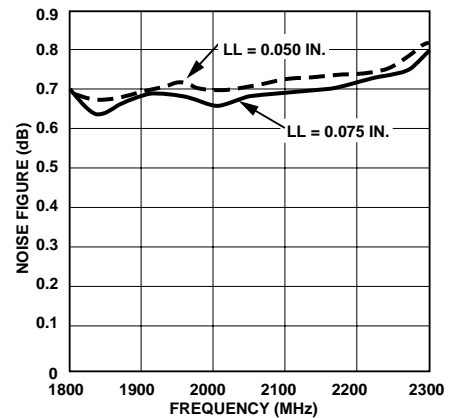


Figure 7. ATF-33143 Amplifier Noise Figure vs. Frequency and Source Lead Length LL .

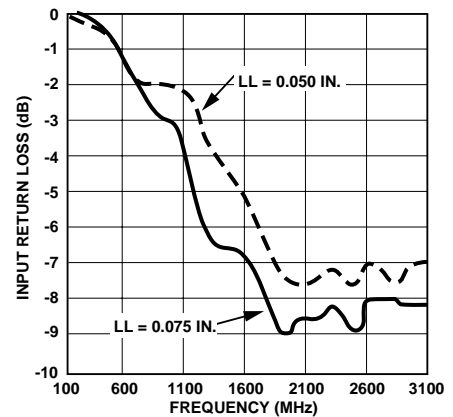


Figure 8. ATF-33143 Amplifier Input Return Loss vs. Frequency and Source Lead Length LL .

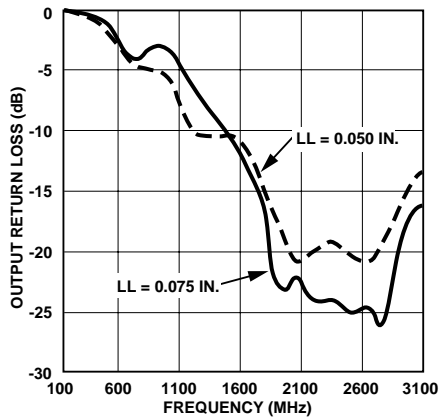


Figure 9. ATF-33143 Amplifier Output Return Loss vs. Frequency and Source Lead Length LL.

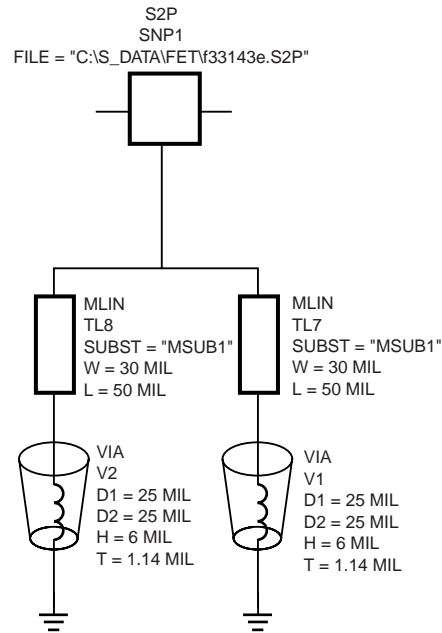


Figure 10. Agilent/EEsof ADS Simulation of the .S2P file with source inductance and vias to bottom groundplane.

Linear Circuit Analysis

The ATF-33143 amplifier circuit was simulated using Agilent Technologies' EEsof Advanced Design System (ADS) software. Due to the complexity of the simulation, the design is presented in three sections. First, the ATF-33143 and its associated source grounding is shown in Figure 10. The S Parameters for the ATF-33143 and other Agilent transistors can be downloaded from the Agilent RF Help Web Site @ <http://www.semiconductor.agilent.com/rf/index.html>

Second, the input matching circuit schematic is shown in Figure 11 and the output matching circuit is shown in Figure 12.

As noted on the data sheet, the ATF-33143 S and Noise Parameters are tested in a fixture that includes plated through holes through a 0.025" thickness printed circuit board. Due to the complexity of de-embedding these grounds, the S and Noise Parameters include the effects of the test fixture grounds.

Therefore, when simulating a 0.031" thickness printed circuit board, only the difference in the printed circuit board thickness is included in the simulation, i.e., $0.031" - 0.025" = 0.006"$. The transmission lines that connect each source lead to its corresponding plated through hole is simulated as a microstripline (MLIN).

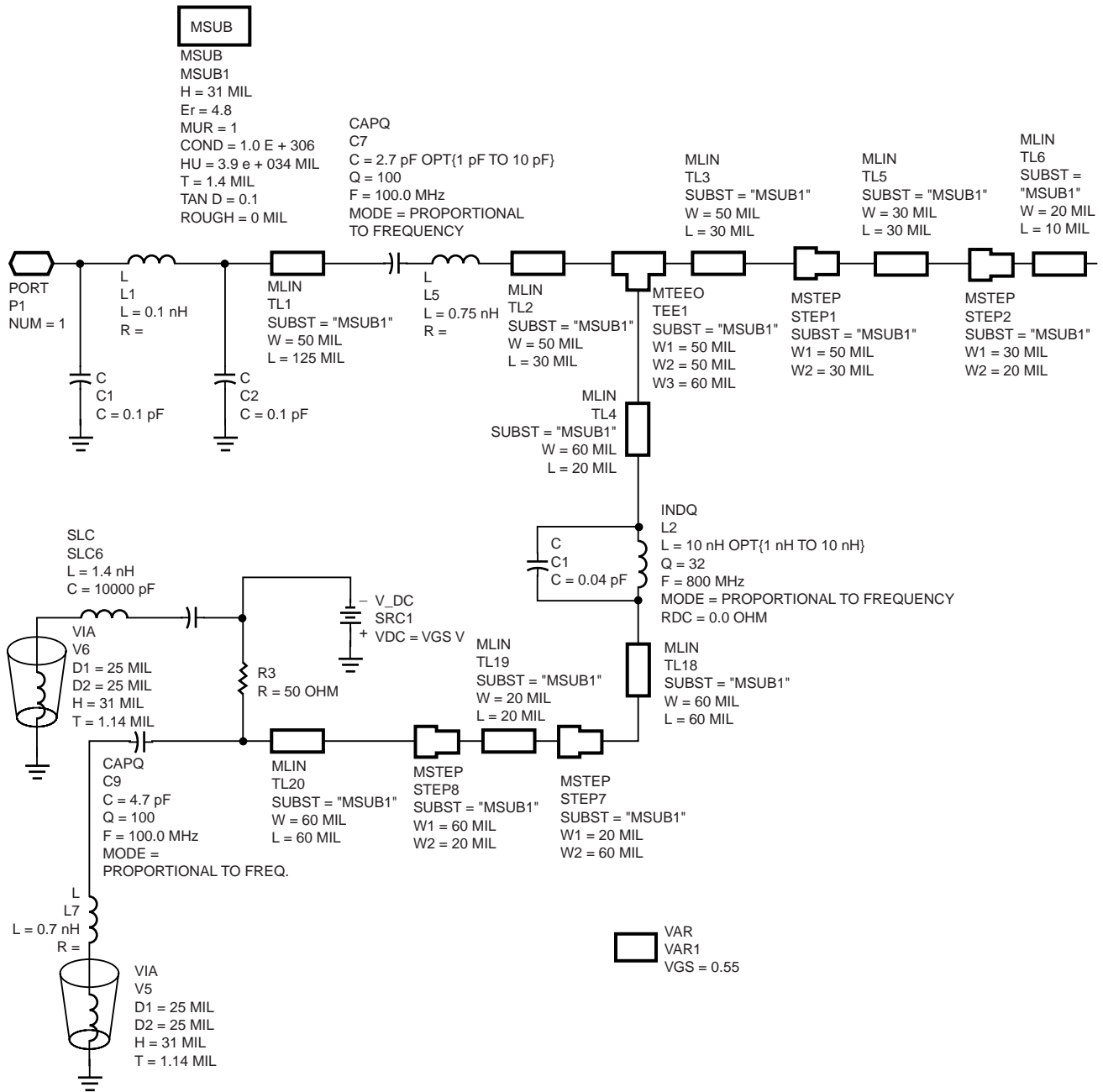


Figure 11. Agilent / EEs of ADS Schematic Diagram of the input impedance matching network for the ATF-33143 Amplifier.

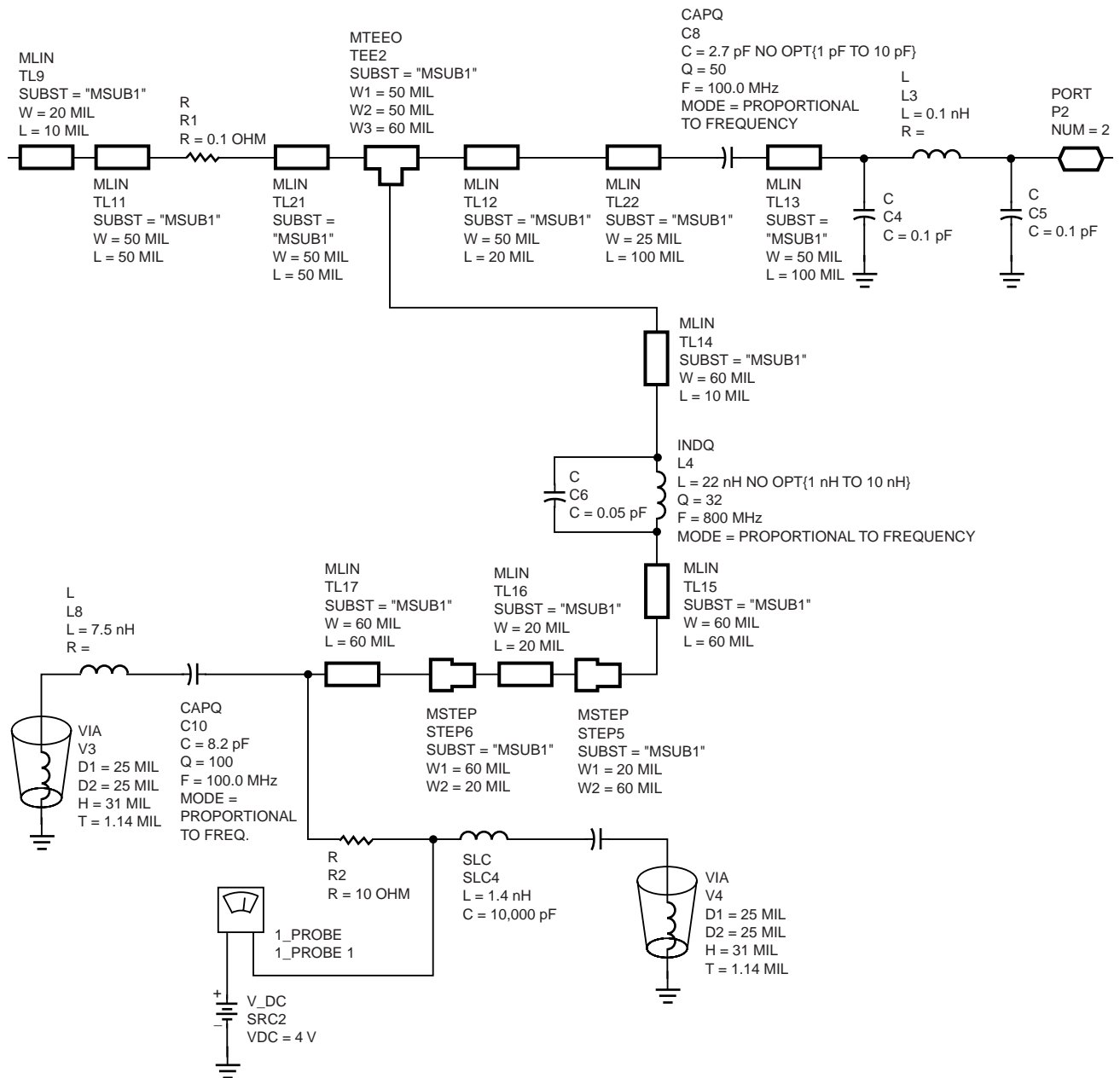


Figure 12. Agilent / EEsof ADS Output Impedance Matching Circuit for the ATF-33143 Amplifier.

The low-pass filter circuit at the input and output connectors models the effects of the end launch SMA connectors used on the demo board. In order to maximize the accuracy of the simulation, the parasitics of all capacitors and inductors have been included in the simulation. Component mounting pads have been modeled as MLINs and junctions have been modeled with MTEEO and MSTEP. The results of the simulation are shown in the following diagrams. It is especially important to insure that the Rollett Stability factor K be greater than 1 over the entire frequency range over which the device has usable gain. See Figure 17.

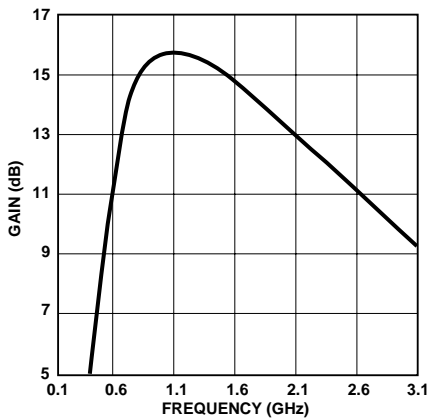


Figure 13. Simulated Gain Performance vs. Frequency.

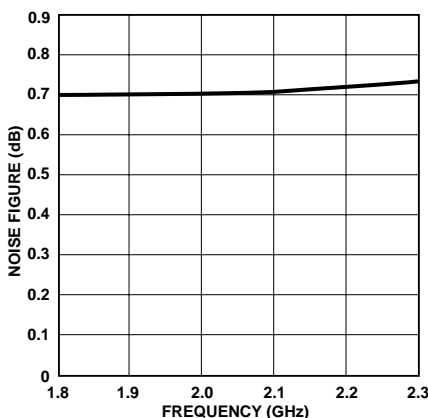


Figure 14. Simulated Noise Figure Performance vs. Frequency.

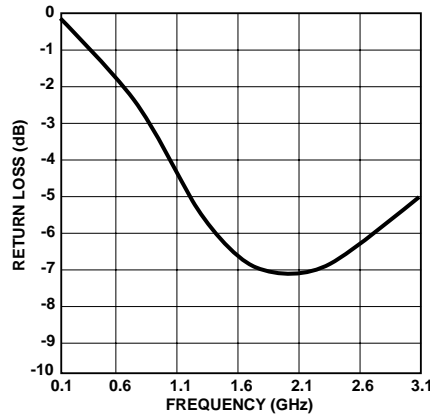


Figure 15. Simulated Input Return Loss vs. Frequency.

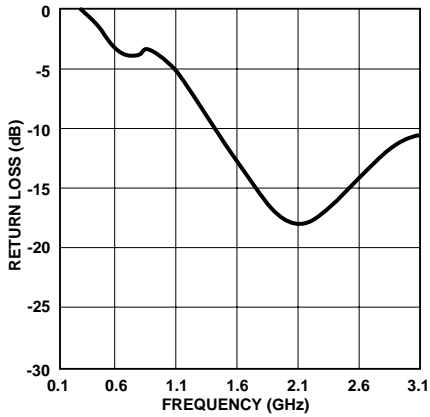


Figure 16. Simulated Output Return Loss Performance vs. Frequency.

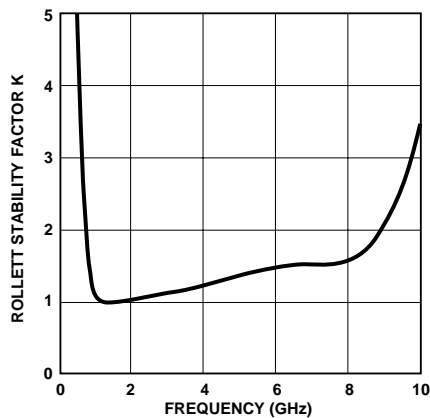


Figure 17. Simulated Rollett Stability Factor K vs. Frequency.

Non-Linear Circuit Analysis

Once the circuit has been optimized using the linear analysis with the published S and Noise Parameters, the circuit can be analyzed using the available non-linear Statz model. The Statz model parameters have been optimized by Agilent to give accurate results at or near the published bias point of $V_{ds} = 4$ V and $I_{ds} = 80$ mA. At a bias point significantly lower than the rated bias point, the model's accuracy diminishes. ADS predicts a nominal +33 dBm output IP3 at 1960 MHz when biased at a $V_{ds} = 4$ V and $I_d = 80$ mA. ADS can be used to make tradeoffs between OIP3 and output return loss.

Conclusion

The ATF-33143 has been shown to yield a very low 0.7 dB noise figure, greater than 13 dB gain and a very high, +32.5 dBm OIP3 at a $V_{ds} = 4$ V and $I_d = 80$ mA. Test results correlate very well to the Agilent/EEsof ADS simulation prediction.

Appendix 1.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain. However, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain rolloff will be gradual and smooth. Adding source inductance begins to add bumps or gain peaks to the once smooth gain roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a very high frequency gain peak in S₂₁ and also shows up as input return loss S₁₁ becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S₂₁ variations in the device.

A wide-band plot of S₂₁ for an amplifier using the 400 micron ATF-35143 amplifier is shown in Figure 18. The ATF-35143 is used in this example because it is more sensitive to source inductance, i.e., high frequency gain is greater with smaller gate width devices. Similar behavior is to be expected using the 800 micron ATF-34143 but to a lesser degree because of its greater gate width. The plot shown in Figure 18 represents an

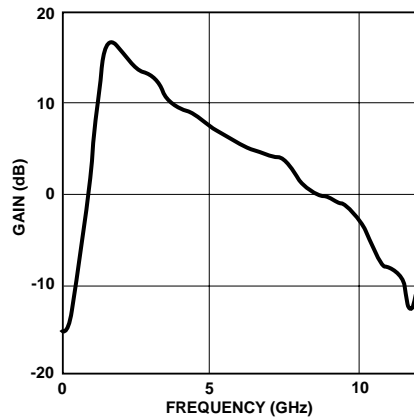


Figure 18. Wide-band gain plot of amplifier using minimal source inductance.

amplifier that uses minimal source inductance and has a relatively smooth gain roll-off at the higher frequencies.

The wideband gain plot shown in Figure 19 is for the same amplifier that uses additional source inductance. Increased source inductance improves low frequency stability by lowering gain. Input return loss will also be improved while noise figure will stay relatively constant. The effect of adding additional source inductance can be seen as some gain peaking in the 6 GHz frequency range. This level of gain peaking shown in Figure 19 is not considered a problem because of its relatively low level compared to the in-band gain.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak at about 6 GHz which could approach 20 to 30 dB. Its effect can be seen in Figure 20. The end result is poor amplifier stability, especially

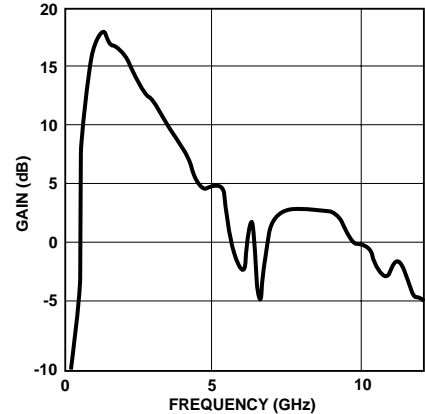


Figure 19. Wide-band gain plot of amplifier with an acceptable amount of source inductance.

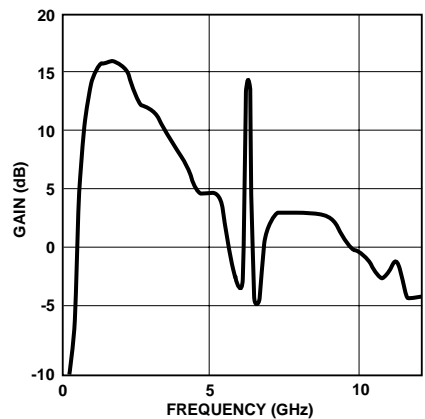


Figure 20. Wide-band gain plot of amplifier with an unacceptable amount of source inductance producing undesirable gain peaking.

when the amplifier is placed in a housing with walls and a cover. Larger gate width devices such as the 800 micron ATF-34143 will be less sensitive to source inductance than the smaller gate width devices and can therefore tolerate more source inductance before instabilities occur. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance.

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